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ELECTRICAL AND PHOTOELECTRIC CHARACTERIZATION OF HETEROSTRUCTURE FETS

MARCH 1996

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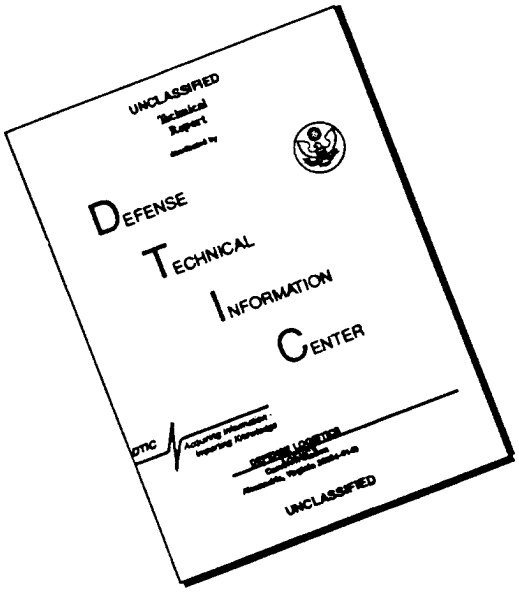

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13. ABSTRACT *(Maximum 200 words)*

This report presents experimental and theoretical studies on Heterostructure Field Effect Transistors (HFETs). Included are dc, rf, and photoelectric measurements. Measurements on devices with very short gate length (200 nm)revealed that the hot electron effects are masked by parasitic effects, specifically source resistance. The hot electron effects were observed using de-embedding techniques. The rf studies revealed that the hot electron effects were not frequency dependant, in agreement with theoretical expectations. An attempt was made to evaluate the increase in electron temperature due to heating by the drain voltage. It was found that the rise in temperature for electrons emitted to the gate is approximately 100 °C. A new photoelectric technique was developed to evaluate non-destructively fully fabricated HFETs. The technique is based on photoemission and conduction (PEC) studies. Intersubband transitions were observed and successfully identified. Furthermore, it was observed that the transistor amplified the photogenerated current due to hole storage effects.

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1 Study of Gate Current and Hot Electron Effects in e/d HFETs

1.1 Introduction

The Institut Für Angewandte Festkörperphysik (IAF, Institute for Applied Solid State Physics) has developed an advanced enhancement/depletion mode GaAs based heterostructure technology with excellent performance. IAF demonstrated digital circuits which operated fully up to 51 GHz clock rates. The aim of this effort was to evaluate and model gate currents, hot electron currents, and subthreshold currents in IAF heterostructure FETs with gate length as small as 0.2 μm. The help and suggestions from many IAF members was appreciated, especially Dr. M. Berroth, Mr. W. Benz, Dr. P. Tasker, Dr. A. Thiede, Dr. J. Braunstein, Dr. C. Moglestue, and Dr. M. Schlechtweg.

Enhancement and depletion mode devices on seven wafers were evaluated. Figure 1 presents schematically the structures of the enhancement and depletion mode devices. The devices on all wafers contained GaAs channels with the exception of wafer DIGSIG 74 which had a InGaAs channel. The gate length of the smallest HFETs was 0.2 μm. Due to the short gate length the device layers must be very thin. Figure 1 presents the typical layer dimensions. The electron confinement layer towards the substrate consisted of a 200 nm AlGaAs, a 1.7 nm GaAs doping layer with 2.5×10^{12} cm^{-2} nominal electron density, and a 5 nm AlGaAs layer. The channel layer was not intentionally doped and was 15 nm thick. A barrier layer followed consisting of a 1.7 nm GaAs electron supply layer sandwiched between two 3.3 nm AlGaAs layers. A 6 nm GaAs cap layer completed the E-mode HFET structure. The D-mode HFET contained additionally a 3 nm AlGaAs and a 7.5 nm GaAs layer. The dopant concentration of both layers was 2×10^{17} cm^{-3}. The wafers AH 96, AH 98,

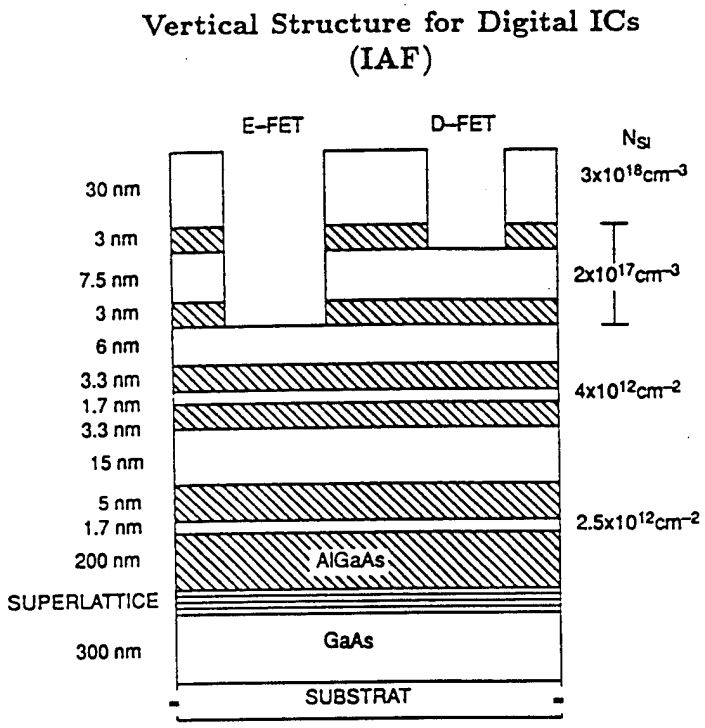


Figure 1. Vertical Structure for Digital ICs

AH 105 and DIGSIG 59 contained this structure. In wafers AH 97, AH 103, and AH 106 the barrier was modified by increasing the 3.3 nm AlGaAs layer on top of the 1.7 nm supply layer to 6 nm and reducing the thickness of the following GaAs layer from 6 nm to 3.3 nm. The DIGSIG 74 wafer contained an $In_{0.2}Ga_{0.8}As$ rather than a GaAs channel layer. The measurements were performed by Mr. W. Benz, using on-wafer probing and a 4145B HP Parameter Analyzer. An existing program was used to extract the following data: Drain and gate currents as function of drain voltage with gate voltage as a parameter, transconductance and drain current as a function of gate voltage for a specific, selectable drain voltage, source and drain resistances, transconductance as a function of

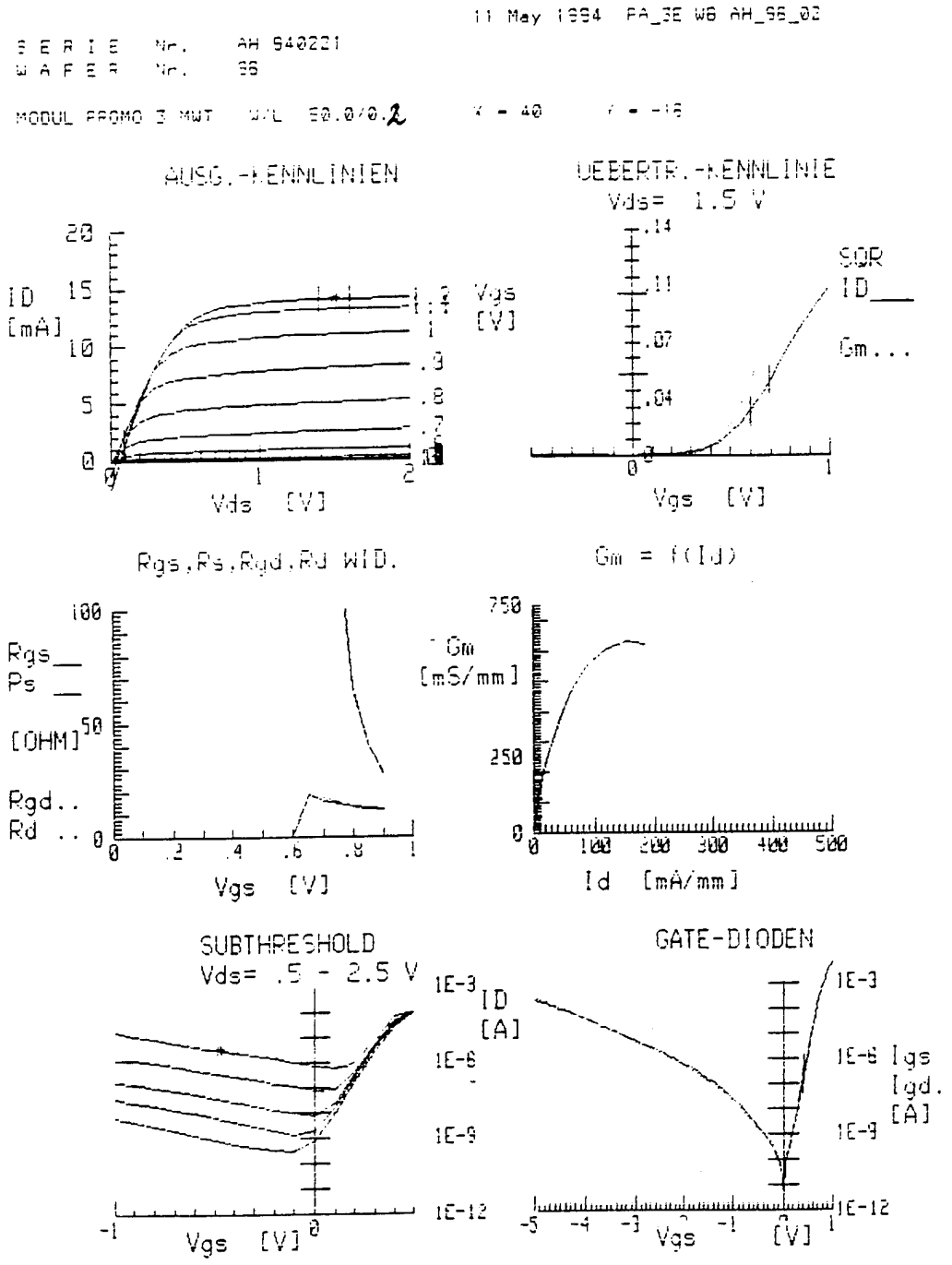
drain current, subthreshold currents as a function of gate voltage and measured at different drain voltages, and gate to source and gate to drain currents as a function of gate voltage.

1.2 DC Characteristics

Figure 2 is a typical representation of measured dc data. The specific enhancement mode device had gate length and gate width of 0.2 and 50 μm respectively. The 6 panels present the drain current Id vs drain voltage Vd characteristics, the transconductance and square root of Id as a function of the gate to source voltage Vgs, source resistance Rs and drain resistance Rd from end-resistance measurements, transconductance vs drain current, subthreshold behavior, and gate current vs gate voltage. The table at the bottom of this figure presents specific data including the threshold voltage and source and drain resistances. The short gate length of these transistors is reflected in the excellent performance parameters such as extrinsic transconductance values in excess of 600 mS/mm.

1.3 Forward Gate Current

Figure 3 presents the gate current of a typical enhancement mode transistor (AH 96 02), measured between gate and source. Figure 3a shows the data in logarithmic and Figure 3b in linear representation. The Figure also contains curves where the data



Ron	=	68.6 Ohm	Idsat	=	14.04 mA	Vth	= .45 [V
	=	3.43 Ohm*mm		=	280 mA/mm	Isub	= 3.26E-6
Rs	=	11.8 OHM	Gm	=	31.684 mS	ns	= 1.57
	=	.59 Ohm*mm		=	634 mS/mm	nd	= 1.6
Rd	=	11.6 OHM	Gds	=	275 uS		
	=	.58 Ohm*mm		=	5.5 mS/mm		

Figure 2. Presentation of DC Parameters

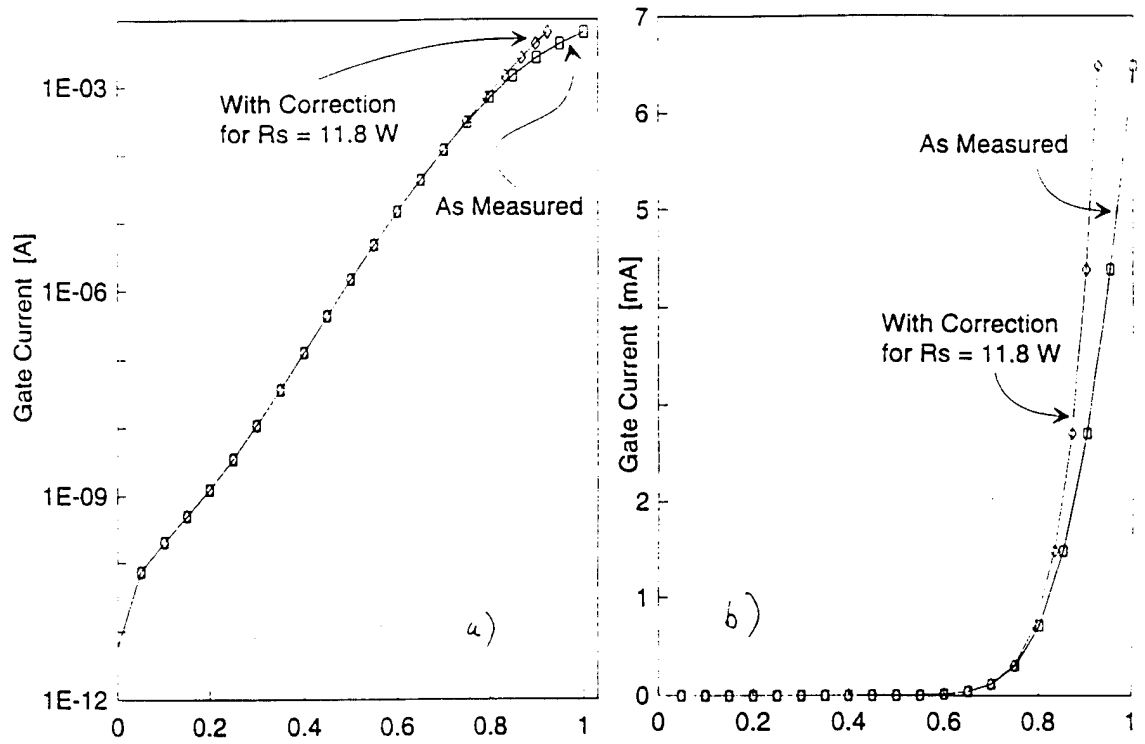


Figure 3. Gate Current of Enhancement Mode HFET

have been corrected for the source resistance. In these curves the gate current is plotted against the internal gate voltage Vgs-Ig*Rs where Ig is the gate current. One observes that in the logarithmic representation the corrected gate current characteristic has a linear behavior at higher current levels, indicating that the source resistance limits the gate current at high current levels. The gate current characteristics observed in these studies are fundamentally different from those measured previously on InGaAs channel HIGFETs presented in Figure 4. The HIGFET gate current characteristic shows two regions: At low gate currents the Schottky barrier controls and limits the gate current. The gate current changes rapidly with gate voltage since the barrier encountered by the electrons in the semiconductor changes directly with gate voltage. The n value in this region is close to one. The IAF data agree with the HIGFET data in this region. At higher gate voltages the

HIGFET gate current is no longer limited by the Schottky barrier but by the heterobarrier which results in a lesser slope in the logarithmic representation. Several structural features can explain the difference in behavior between the IAF and HIGFET devices. The longer gate length of the HIGFET allowed for a thicker barrier layer, the InGaAs pseudomorphic channel increased the height of the heterobarrier, the barrier was undoped, and a uniform barrier layer was used.

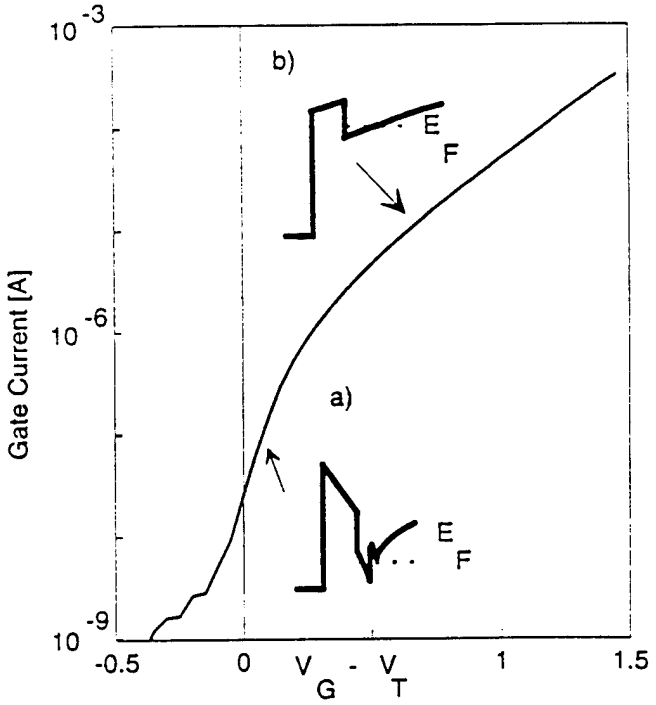


Figure 4. Gate Current Characteristic of HIGFET

Figure 5 presents the gate current vs intrinsic gate voltage Vg' of the enhancement mode HFET AH 105 02 both in linear and logarithmic representation. The source resistance Rs was chosen to be 28.4 Σ. The gate voltage was scanned from 0 to 1.2 V and the drain voltage from 0.5 to 2 V. The Figure shows that all data points are located on one curve independent of drain voltage. This result suggests that the gate current is made up

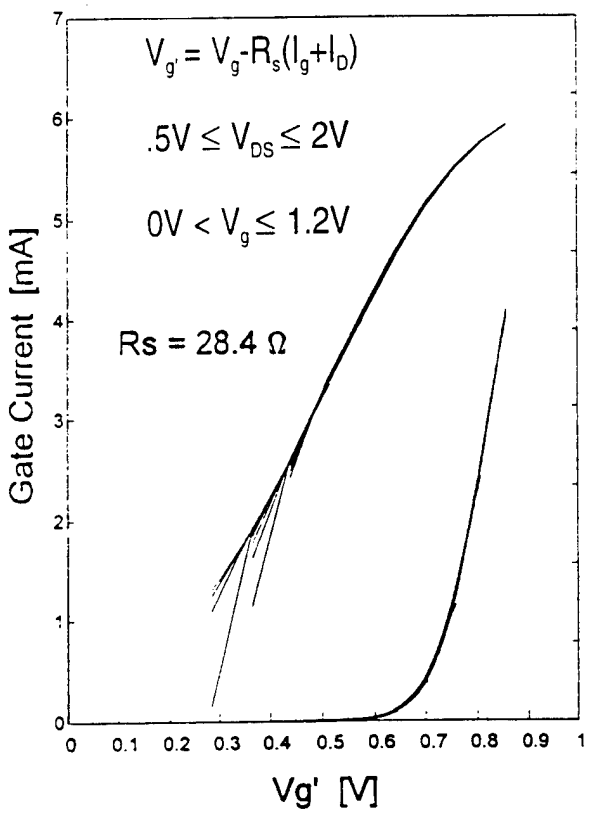


Figure 5. Gate Current vs Intrinsic gate voltage for different drain voltages.

of two components, the gate to source and the gate to drain currents. Since the gate to drain potential is at least 0.5 V smaller than the gate to source potential, the gate to drain current is significantly smaller than the gate to source current and is negligible. Note from this Figure and also from previous figures that the gate current depends exponentially on the gate voltage and small changes in gate voltage lead to large changes in gate current. These findings are typical for enhancement mode transistors. Best n values for both enhancement and depletion mode devices are 1.5 and typical values between 1.5 and 2.

In previous studies hot electron effects were observed due to the acceleration of the channel electrons by the drain potential. The dependance of the gate current on the drain

voltage reveals the hot electron effect and Figure 6 presents an example which was obtained on a HIGFET. The observed increase in gate current with increasing drain

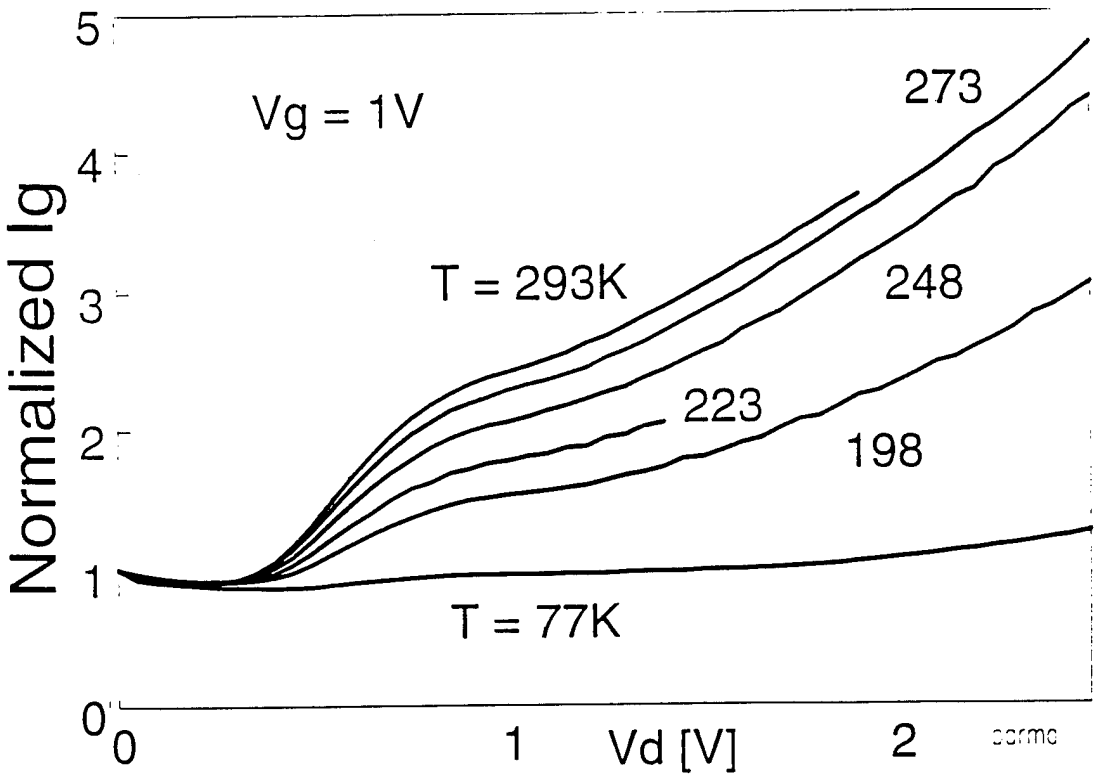


Figure 6. Normalized Gate Current.

voltage is caused by heating of the electrons by the drain potential. Figure 7 presents the gate current vs drain voltage, measured at different gate voltages for a typical IAF HFET. The curves indicate a rapid decay in gate current with drain voltage followed by a marginal increase. No electron heating effects are evident from this figure. The rapid decrease in gate current is caused by the source resistance Rs. Due to the increasing source current the voltage drop across this resistance increases and consequently the intrinsic gate voltage (Vgs-Is*Rs) decreases with drain voltage, resulting in the observed decrease

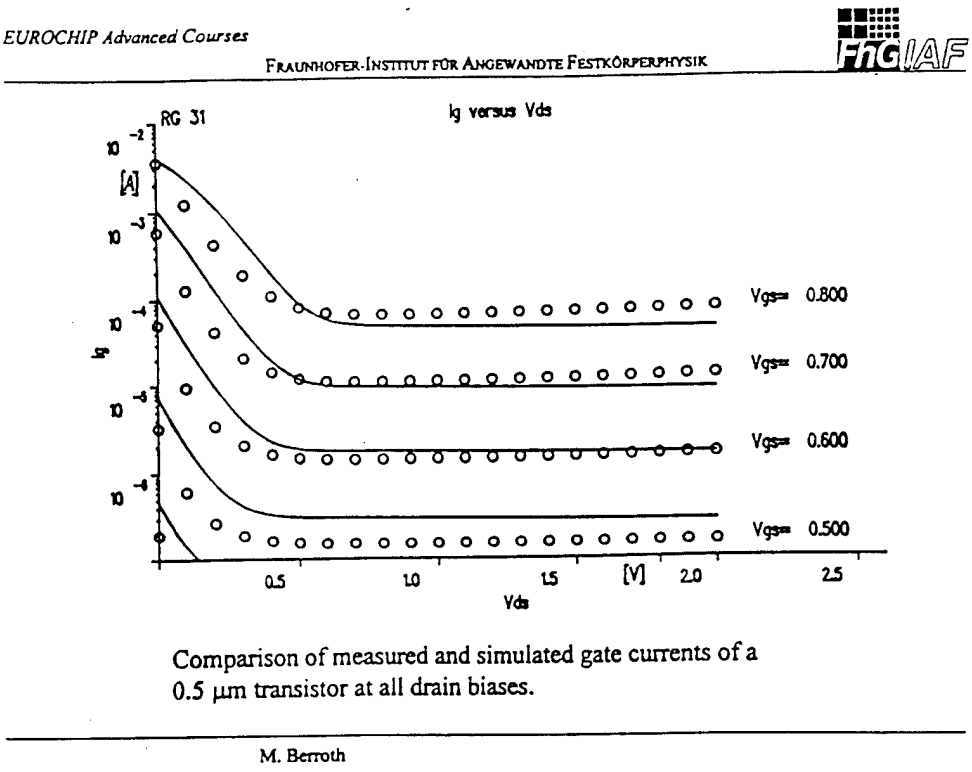


Figure 7. Gate Current vs Drain Voltage of IAF HFET

in gate current. The simulated gate current curves in Figure 7 take the source resistance into account.

In Figure 8 the gate current of a depletion mode HFET is plotted in dependance of the intrinsic gate to source voltage with drain voltage as a parameter. One observes that the gate current depends not only on the intrinsic gate voltage but also on the drain voltage. This behavior is different from that observed for the enhancement mode FET, shown in Figure 5 where the gate current was independent from the drain voltage. One further observes that over a large gate intrinsic voltage regime the gate current measured at Vds = 2 V is larger than that at 0 V, indicating a hot electron behavior, similar to that observed on HIGFETs. To better observe the hot electron behavior, the gate current must

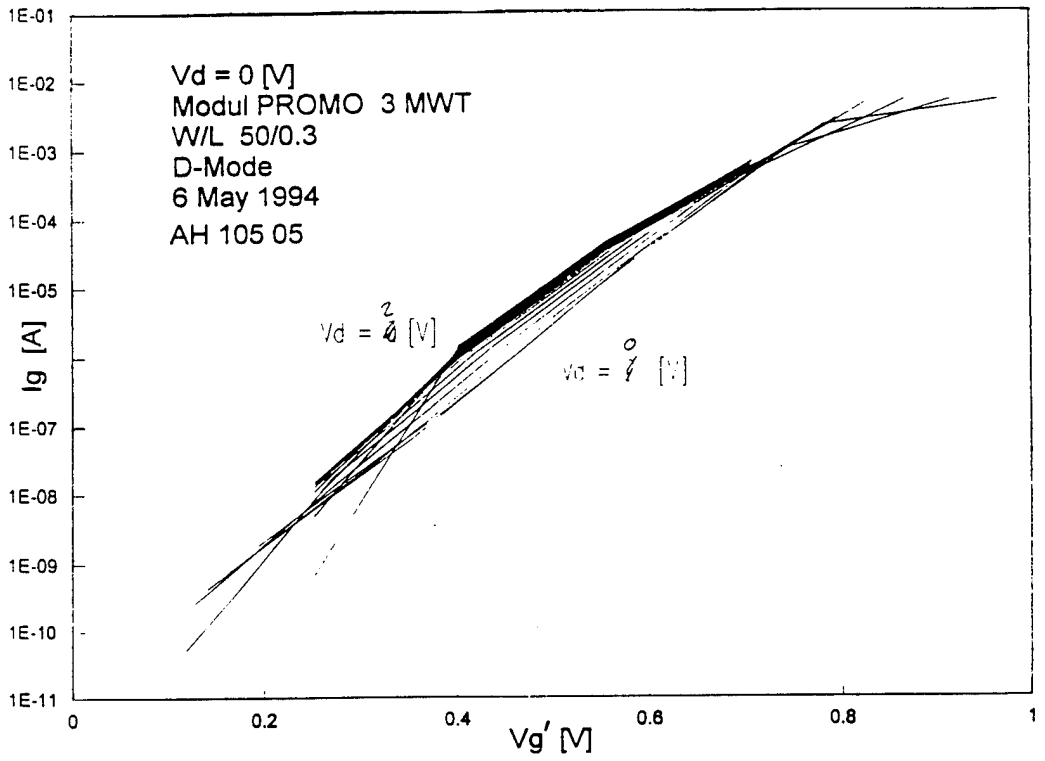


Figure 8. Gate Current vs Intrinsic Gate Voltage for Depletion Mode HFET

be plotted as a function of drain voltage with the intrinsic rather than extrinsic gate voltage as a parameter. The gate current data for specific intrinsic gate voltage values were obtained by interpolating the experimental data. The gate current is an exponential function of the gate voltage as shown in Figures 5 and 8 and consequently the interpolation was performed in logarithmic representation.

Figure 9 presents the gate current and the normalized gate current of two depletion mode HFETs, AH 105 05 and AH 105 06 for an intrinsic gate voltage of 0.6 V. These curves show the same hot carrier effects as those observed on HIGFETs. After an initial decrease in gate current one observes an increase and the final current is well above the its level at zero drain voltage. The device AH 105 06 shows an increase by a factor of three. The gate currents depend exponentially on applied and intrinsic potentials and are more difficult

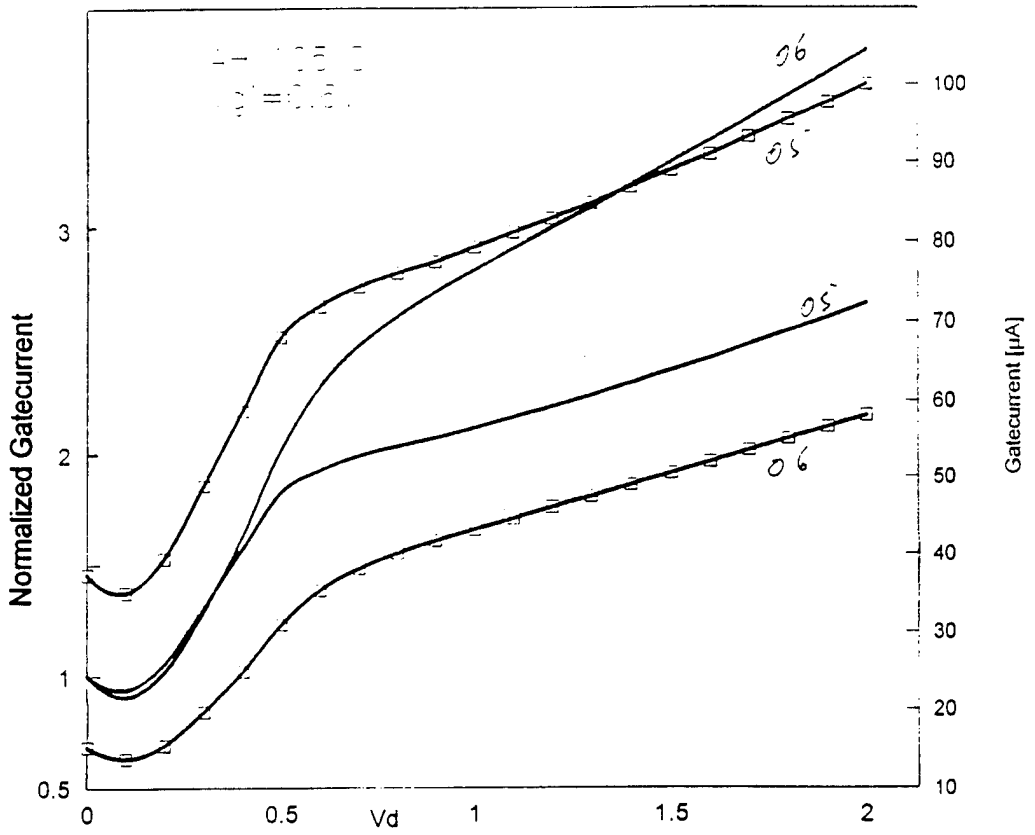


Figure 9. Gate current dependance on drain voltage for a 0.6 V intrinsic gate voltage

to control than for instance the drain current. This is the cause for the large variance in gate currents for the two devices.

In both Figures 8 and 9 the source resistances were obtained from the end-resistance measurements as recorded in Figure 2. It is very difficult to determine the correct source resistance. In the end-resistance technique part of the channel resistance is included and in general this resistance value is too large. In Figure 10 the sensitivity of the gate currents to the chosen source resistance is evaluated for the device AH 105 05 at an intrinsic gate voltage of 0.7 V. The source resistance obtained from end-resistance measurements was 10.7 Σ for the 50 µm gate length HFET. This figure indicates that the gate current for a specific intrinsic gate voltage is critically dependant on the selected source resistance and a more accurate determination of the source resistance is needed. To eliminate the

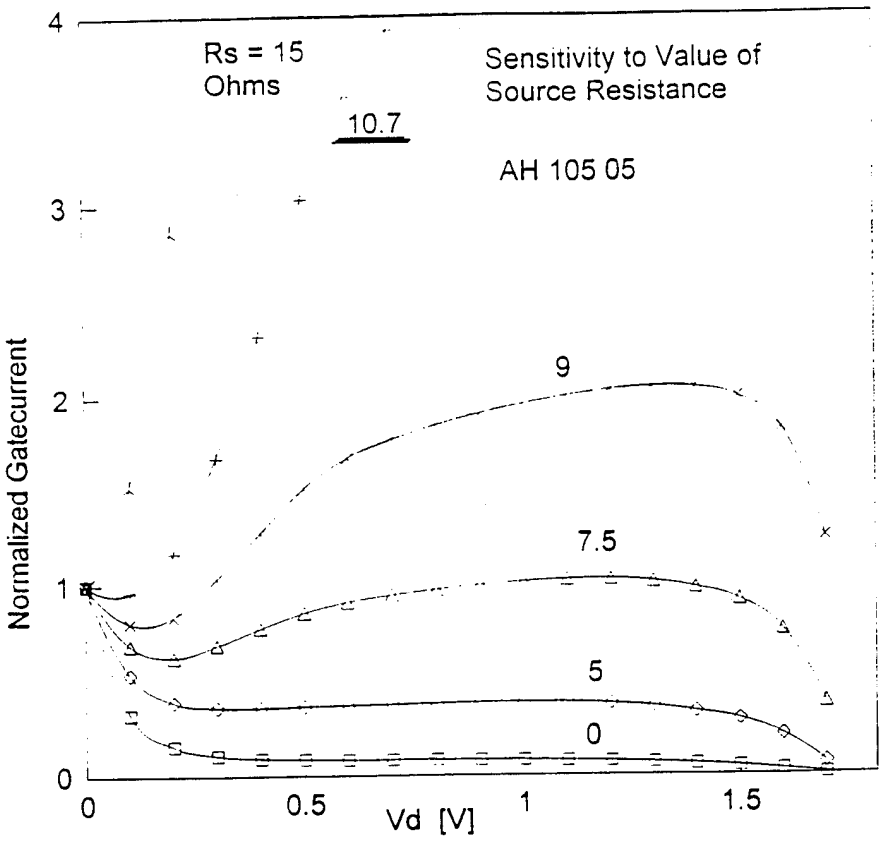


Figure 10. Gate Current dependance on Drain Voltage for Various Source Resistance Values

contribution by the channel resistance, the source resistances values obtained from end-resistance measurements for several devices are plotted against their gate length (Figure 11) and the linear fit to the data points is extrapolated to zero gate length, resulting in a source resistance of 27.75 Σ for the 20 μm wide devices. The source resistance can also be derived from TLM measurements and Figure 12 presents a typical example for the wafer AH 105. A sheet resistance value of 283.23 Σ/o and a contact resistance value of 0.1652 Σ-mm was found. These data translate into a sheet resistance value of 14.16 Σ and a contact resistance value of 8.26 Σ for a total source resistance Rs of 22.42 Σ for the 20 μm wide HFETs with 1 μm source to gate spacing. This value agrees with the previously

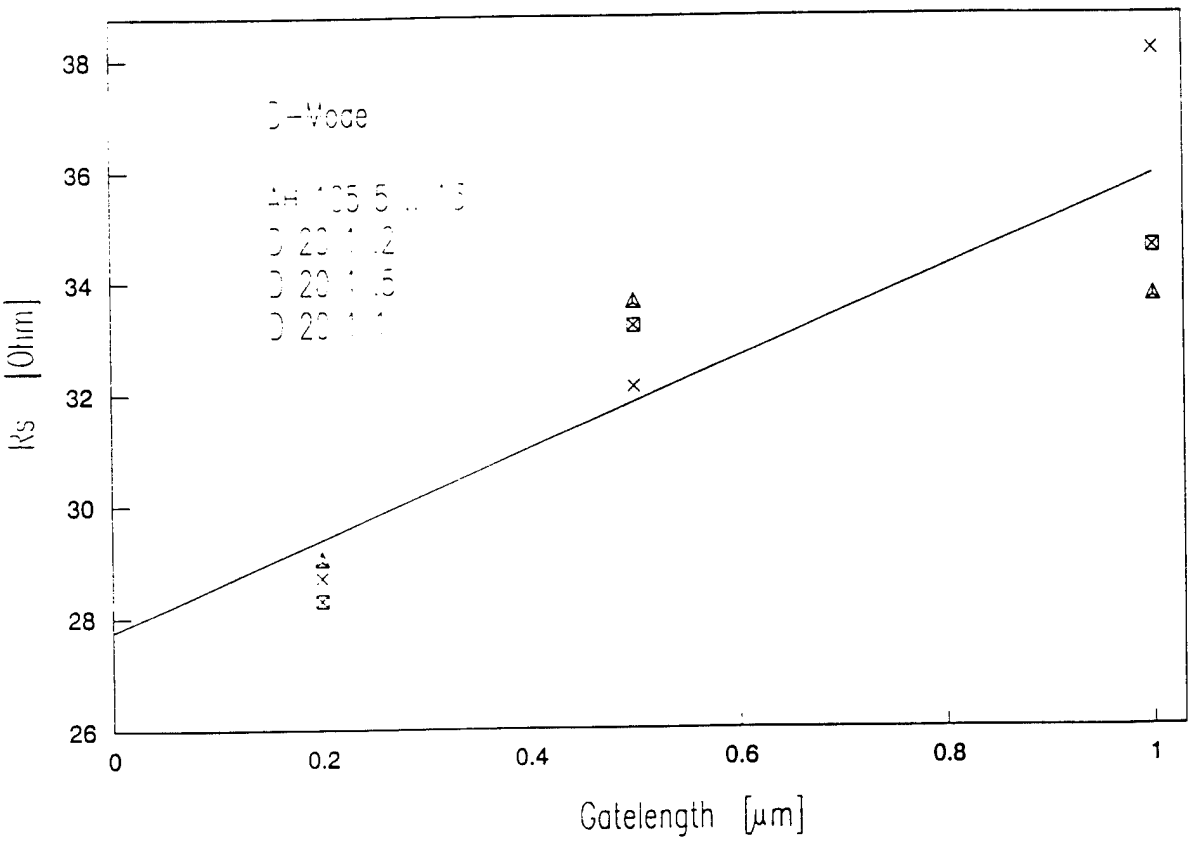


Figure 11. Source Resistance vs gate length

determined value of 27.75 Σ within 20%. Figures 13 presents device data corrected for the resistance values 27.75, obtained from the end-resistance data, and 20 Σ, a 10 % smaller value than that obtained from TLM measurements. Both sets of adjusted device data show carrier heating effect as evidenced by the increase in gate current with drain voltage. Of significance is that the carrier heating effect increases with a decrease in gate length. The normalized gate current graph for Rs = 27.75 Σ shows current increase factors of approximately 5.7, 2.9, and 2 for gate lengths of 0.2, 0.5, and 1 µm respectively. This finding is significant since two opposing effects take place as the gate length is reduced. The electric field in the channel is increased as the channel length is reduced, resulting in an increase in electron temperature and enhanced emission. Yet the carrier emission

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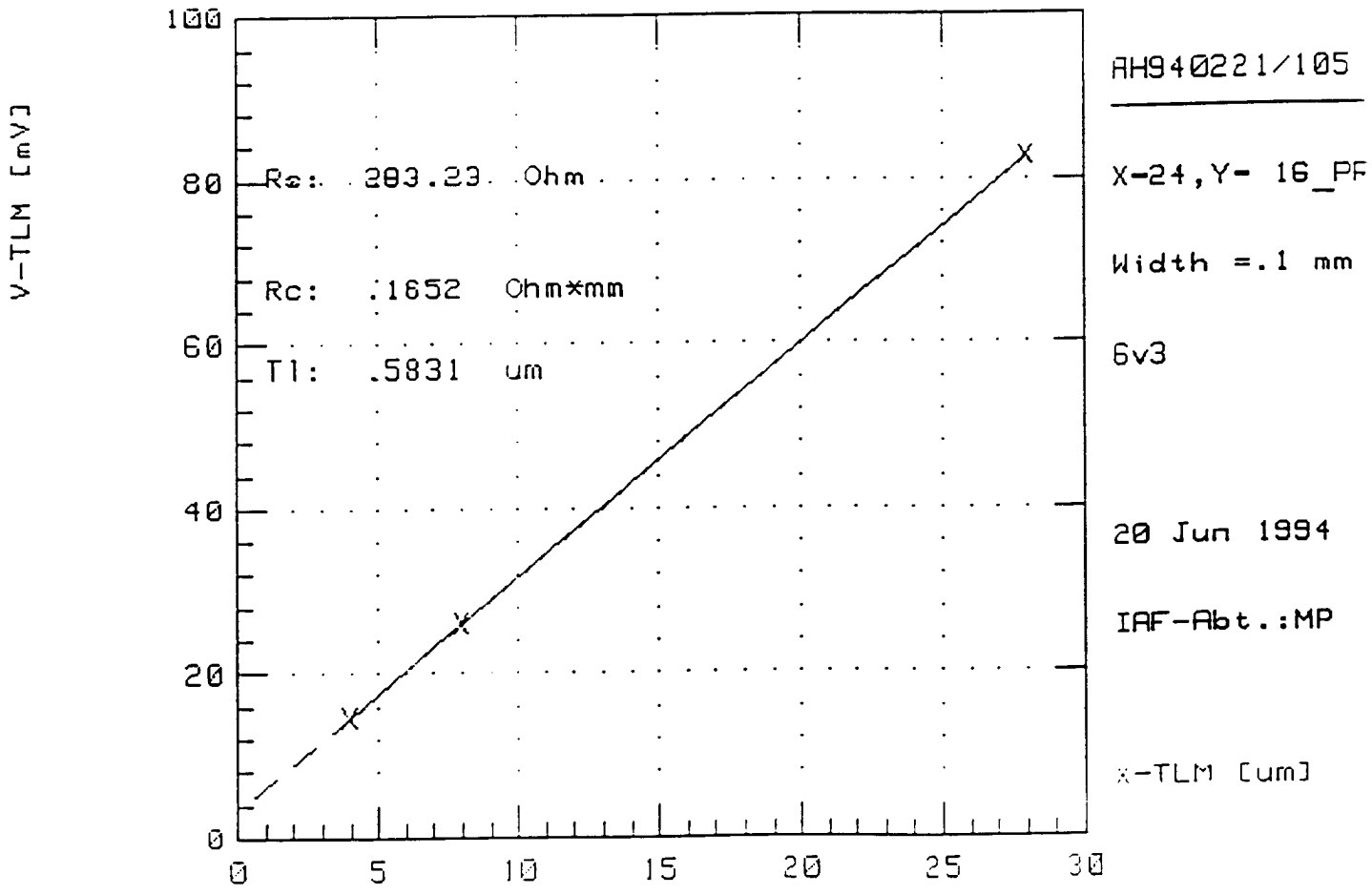

Figure 12. TLM Resistance Evaluation

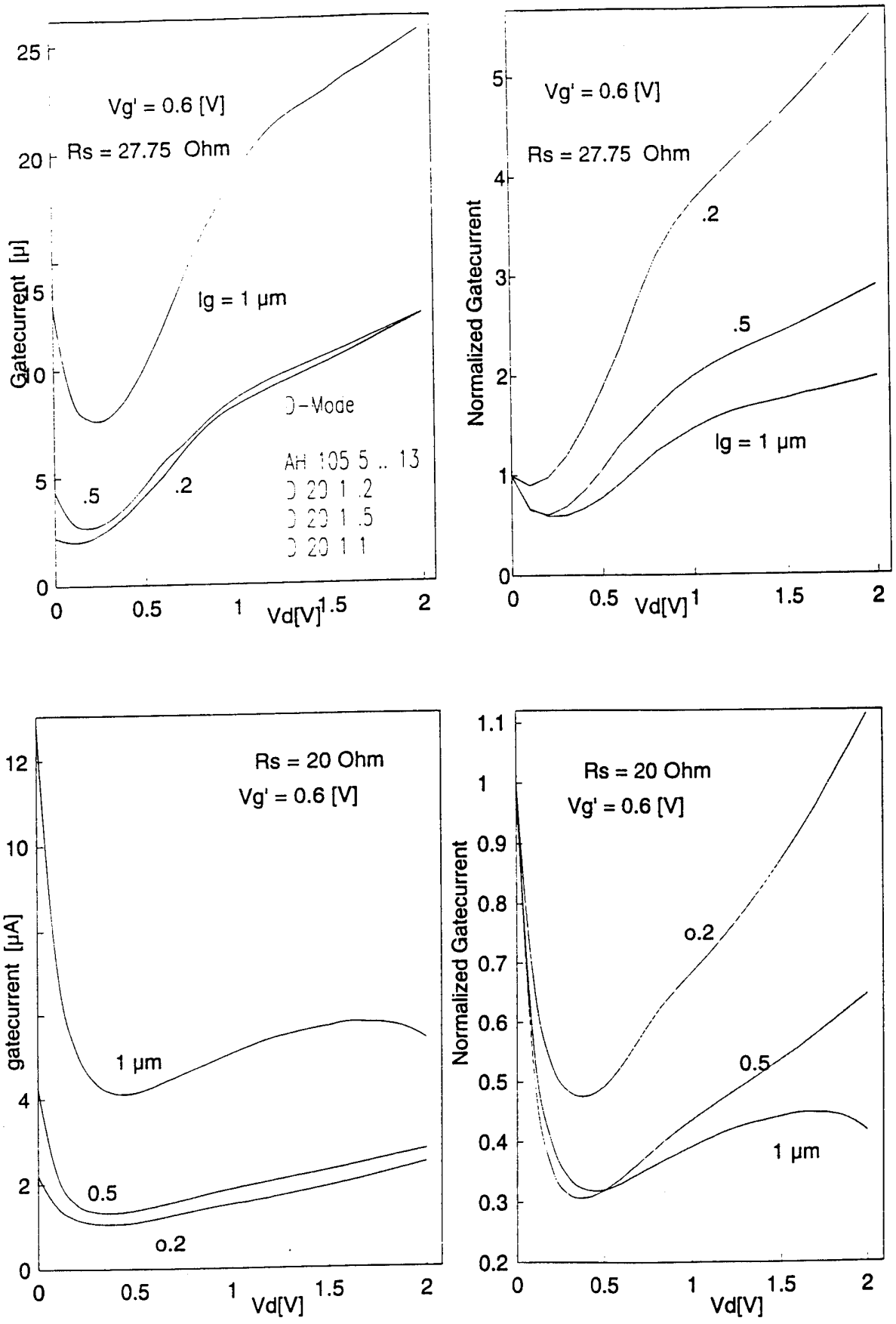

Figure 13. Gate Current and Normalized Gate Current for 0.2, 0.5, and 1 µm gate length. Rs and Vg' are listed

requires scattering events to change the momentum of the electron from a direction parallel to one orthogonal to the channel. The channel length may become comparable to the scattering length for very short channels. Hence one expects a decrease in hot electron emission with decreasing gate length in this regime of operation. The experimental evidence of increased emission of heated carriers clearly proves that the reduction of scattering events with decrease in gate length is of lesser importance than the increase in electric field, which results in increased electron temperature. Also significant is that the data adjusted with a source resistance value of 20 Σ still show the carrier heating effect. This resistance value is smaller than the actual source resistance, clearly proving that the carrier heating effect exists in the devices studied and this effect does not a result from the selection of source resistance values which were too large.

Figures 14 and 15 present gate current characteristics of $In_{0.2}Ga_{0.8}As$ Channel HFETs (DIGSIG 74) and these data are compared to similar HFETs with GaAs channel (DIGSIG 59). Since the height of the heterobarrier is larger in devices with InGaAs channels (by approximately 200 meV) than those with GaAs channel the appearance of the two gate current regimes controlled by Schottky and heterobarriers was of interest. Figures 14 and 15 do not reveal these two current regimes. The absents of the region where the heterobarrier controls and limits the gate current is caused by the doping of the barrier layer. The comparison between the GaAs and InGaAs channel devices reveals that the gate current in the latter devices is smaller. The large difference in gate currents between the two types of depletion mode devices (Figure 14) is probably caused by the doping of the top layers of the InGaAs devices rather than by differences in the channel

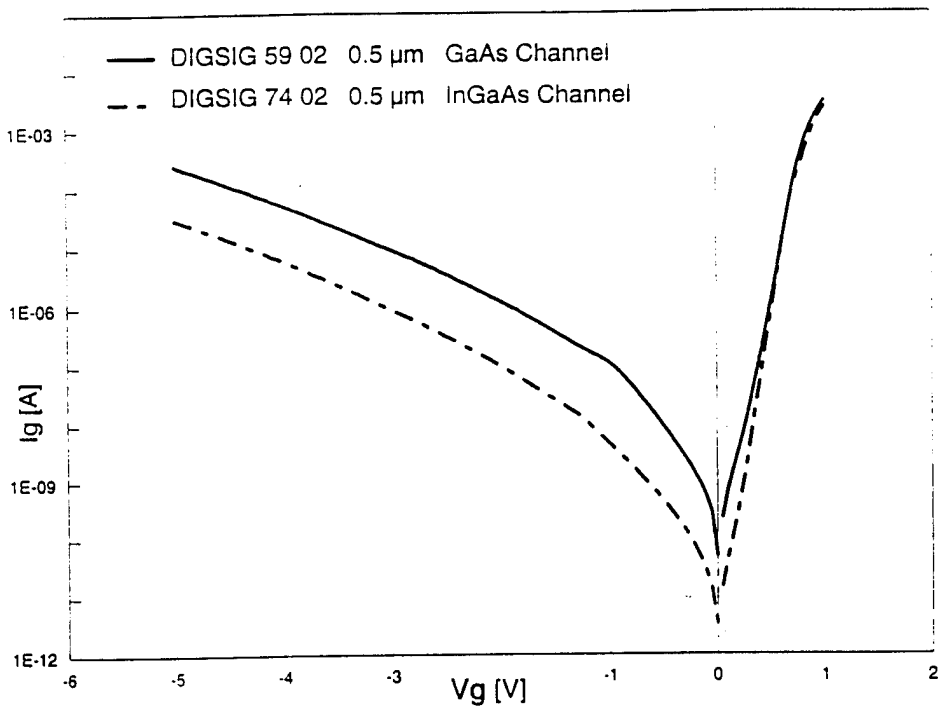

Figure 14. Gate Current vs Gate Voltage Characteristics of InGaAs Channel Depletion Mode HFET characteristics. Especially the difference in the reverse characteristics is large where the Schottky barrier controls the current.

In Figure 16 the normalized gate current vs intrinsic drain voltage for an enhancement mode InGaAs channel HFET is shown. It is interesting to note that the carrier heating effects are seen in InGaAs channel enhancement mode HFETs in contrast to the GaAs channel devices where these effects were only seen in depletion mode devices. One reason for the appearance of carrier heating effects in enhancement mode devices may be that the mobility and the electron velocity in the InGaAs channel devices is larger than in GaAs channel devices. However the carrier heating effect could also be caused by changes in the structure such as the missing doping in the topmost layers. It is important to realize that the threshold and pinchoff voltages in the InGaAs channel devices are more

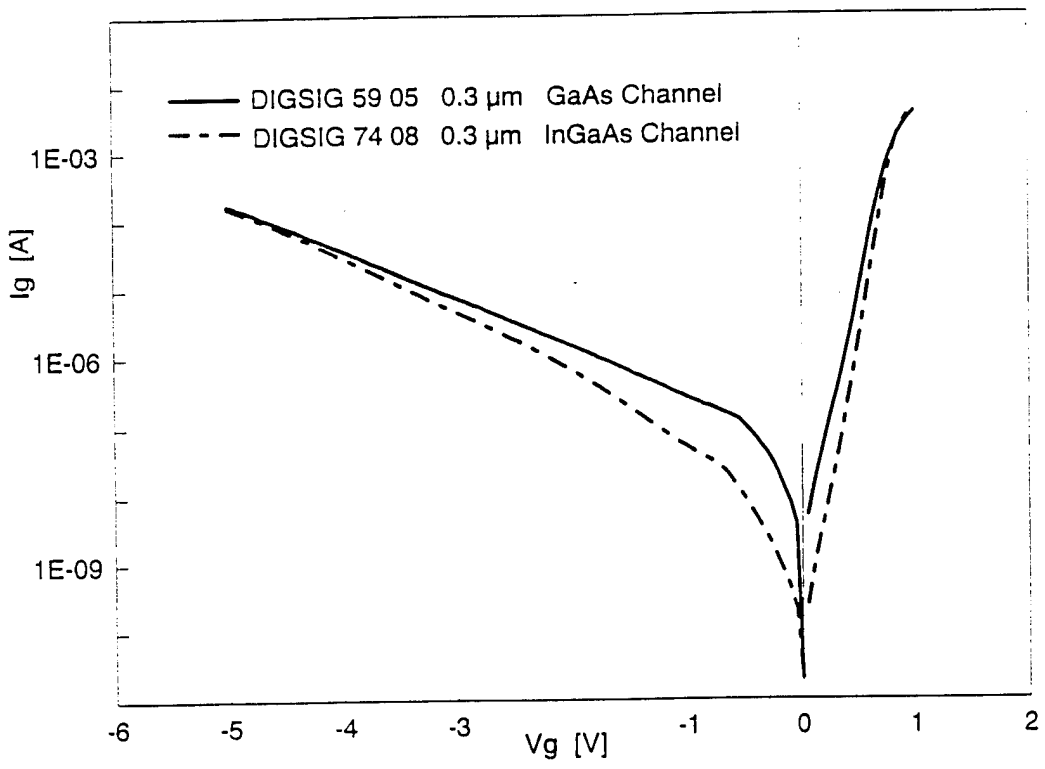

Figure 15. Gate Current vs Gate Voltage for InGaAs Channel E-HFET

negative than those in GaAs channel transistors. This is expected due to the smaller bandgap of InGaAs in comparison to GaAs and the larger conduction band discontinuity.

1.4 Gate Currents Under Reverse Bias

The lower right panel in Figure 2 presents the gate current under forward (positive) and reverse bias conditions on a logarithmic scale. A straight line behavior is observed at larger voltages. Figure 17 presents the distribution of the gate current at a bias voltage of -5 V for many devices measured. Both gate currents between gate and source and between gate and drain are plotted for the wafers AH 96, AH 98, AH 103, AH 105, and AH 106.

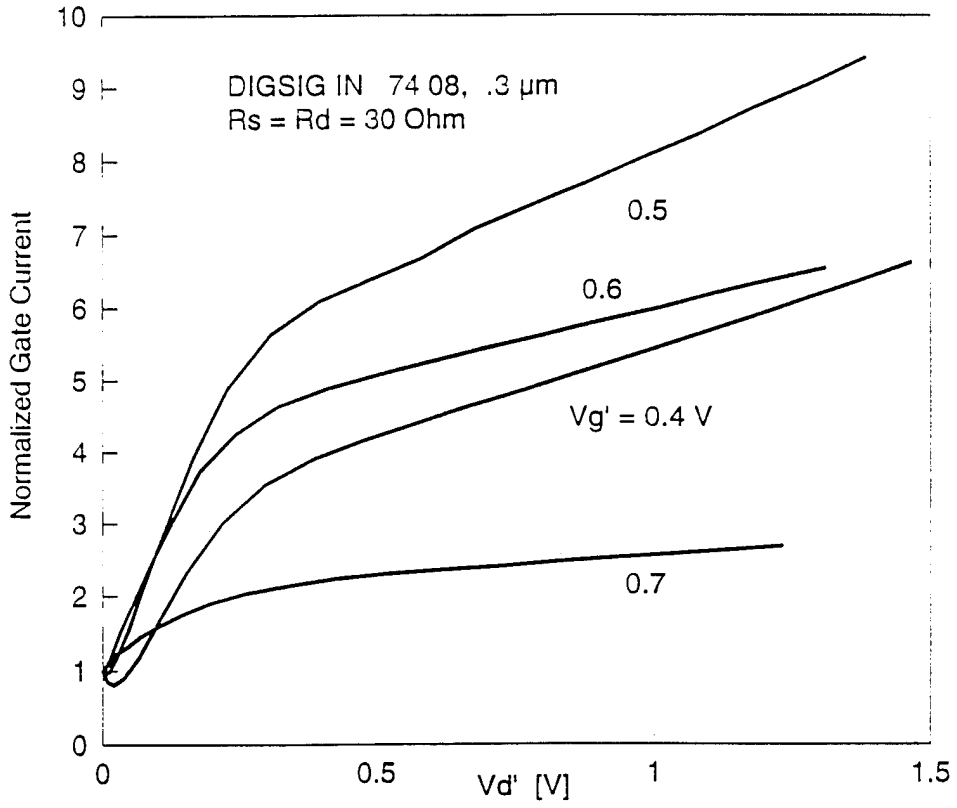

Figure 16. Normalized Gate Current vs Intrinsic Gate Voltage with Intrinsic Gate Voltage as Parameter InGaAs Channel E-HFET

The first two transistors in each group are enhancement mode devices and the latter ones depletion mode transistors. Since gate currents are a strong function of the fields in the structure, one observes wide scatter of the data. No difference between wafers nor between transistor type are apparent. Note that wafers AH 103 and AH 106 had a thicker AlGaAs barrier layer than the remaining wafers. The linear regions of these reverse gate current regions were approximated by straight lines and Figures 18 and 19 present the slopes and the y-axis intercepts of these lines respectively. Again no differences in these parameters for the enhancement and depletion mode FETs nor for the wafers with increased AlGaAs barrier layers is identifiable.

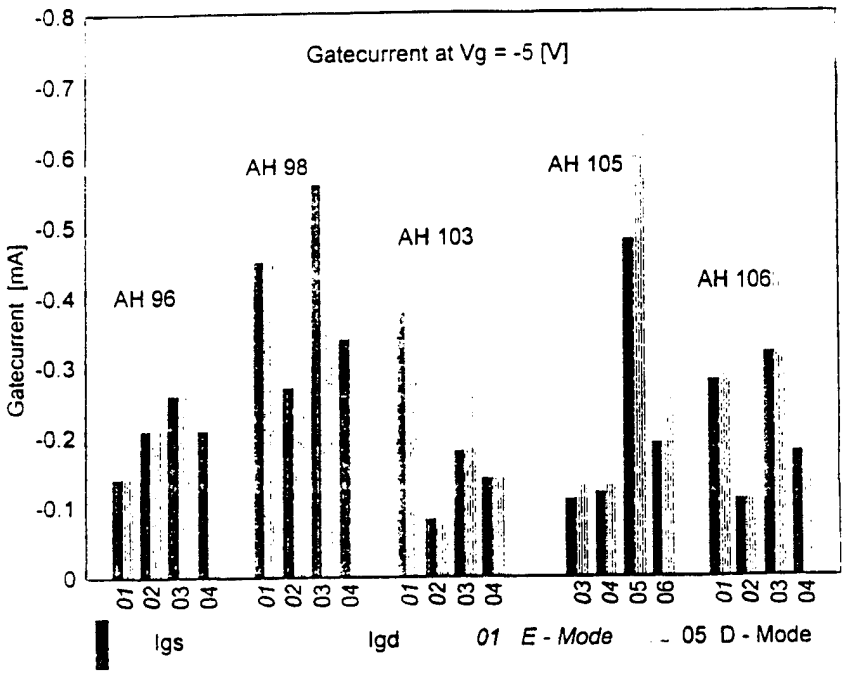

Figure 17 Reverse Gate currents at Vg = -5 V for 5 wafers, enhancement and Depletion HFETs

In Figure 20 the gate current as a function of Vg-Vd is plotted. Note that a positive drain voltage represents a negative gate potential to the gate to drain diode. In this representation the gate currents depend on gate voltage rather than on the gate to drain potential and the curves for the different gate voltage do not coincide. In the right side part of this figure the curves could be overlapped by multiplying the currents for each gate voltage with a factor shown in this graph. This procedure represents a way on modeling the reverse gate currents. The scatter of the gate current data as shown in the earlier figures however makes such an approach unrealistic.

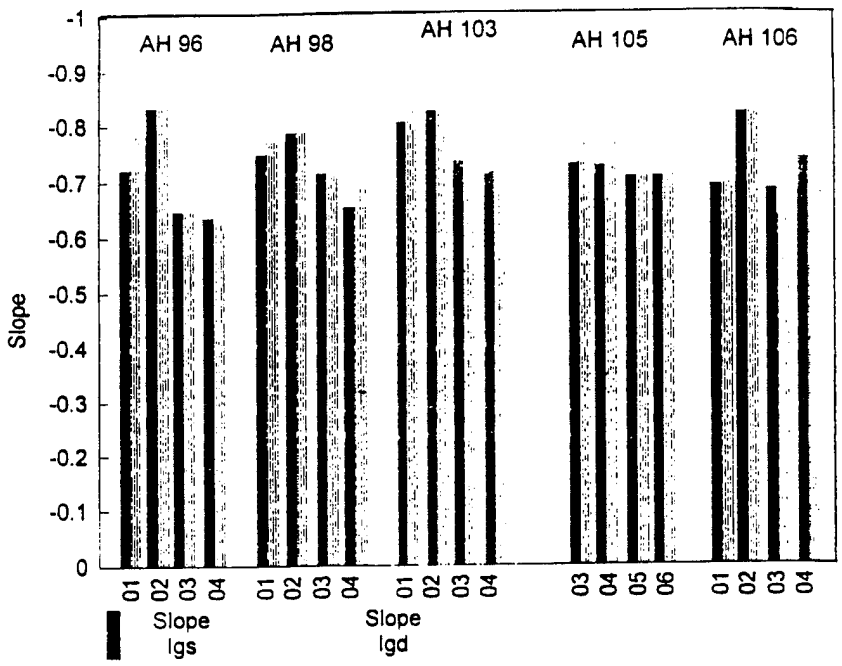

Figure 18 Slope of Reverse Gate Current Approximation for 5 Wafers, Enhancement and depletion Mode HFETs

1.5 RF Measurements

There are several effects that can account for the increase in gate current with drain voltage. As an example the drain potential could increase the surface leakage currents. Since the gate current is similar to the current in a Schottky diode this current must not vary with frequency. In contrast, many of the parasitic currents should be slow. Hence it is important to compare dc and rf gate current data. Since the gate currents are often very small while the capacitance values are still quite large, these measurements must be performed at "moderate" frequencies. A HP 8751A Network Analyzer was used with a frequency range of 5 Hz to 500 MHZ in conjunction with a HP 87511A 100 kHz to 500 MHZ S-Parameter Test Set and the measurements were performed at the latter frequency

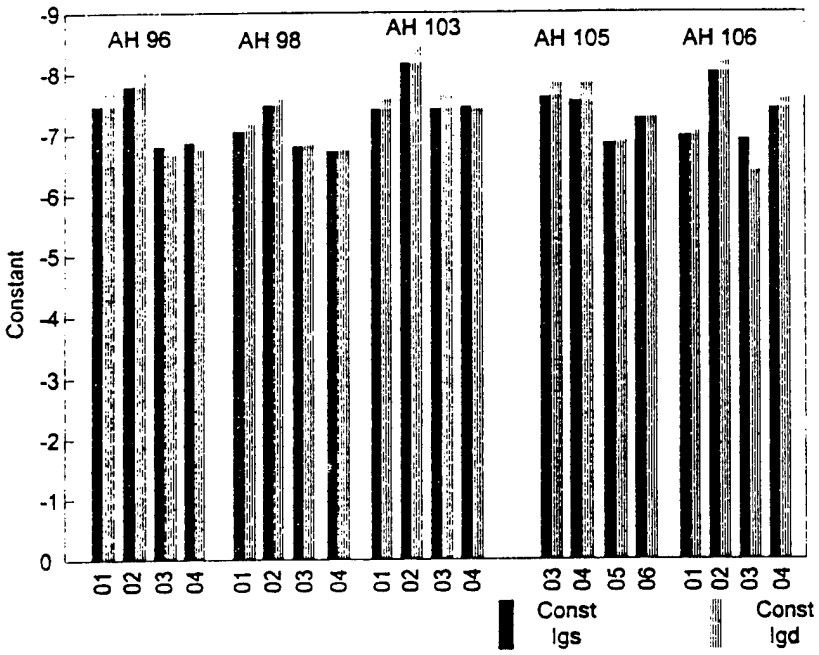

Figure 19 Intercept of Linear Approximation of Reverse Gate Current (Logarithmic Scale)

range. The voltages were supplied to the transistor by a 4155A Semiconductor Parameter Analyzer. The 4155A was also used to perform DC measurements on the same transistor, using Cascade probes. The rf data represent a differentiation of current voltage characteristics and these data can be compared to dc data by integrating the rf data or the dc data can be differentiated and these values then can be compared to the rf characteristics. Here the latter approach was chosen. Figure 21 presents both dc and rf data on a depletion mode HFET from wafer AH 105. Shown are d(Ig)/d(Vd) characteristics, plotted on a logarithmic scale as a function of Vd. The upper panel represents positive slopes while the lower panel negative ones. Figure 7 indicates that at low drain voltages the gate current decreases with drain voltages. Consequently the derivative of these curves yield negative slopes as indicated in Figure 21. In the s

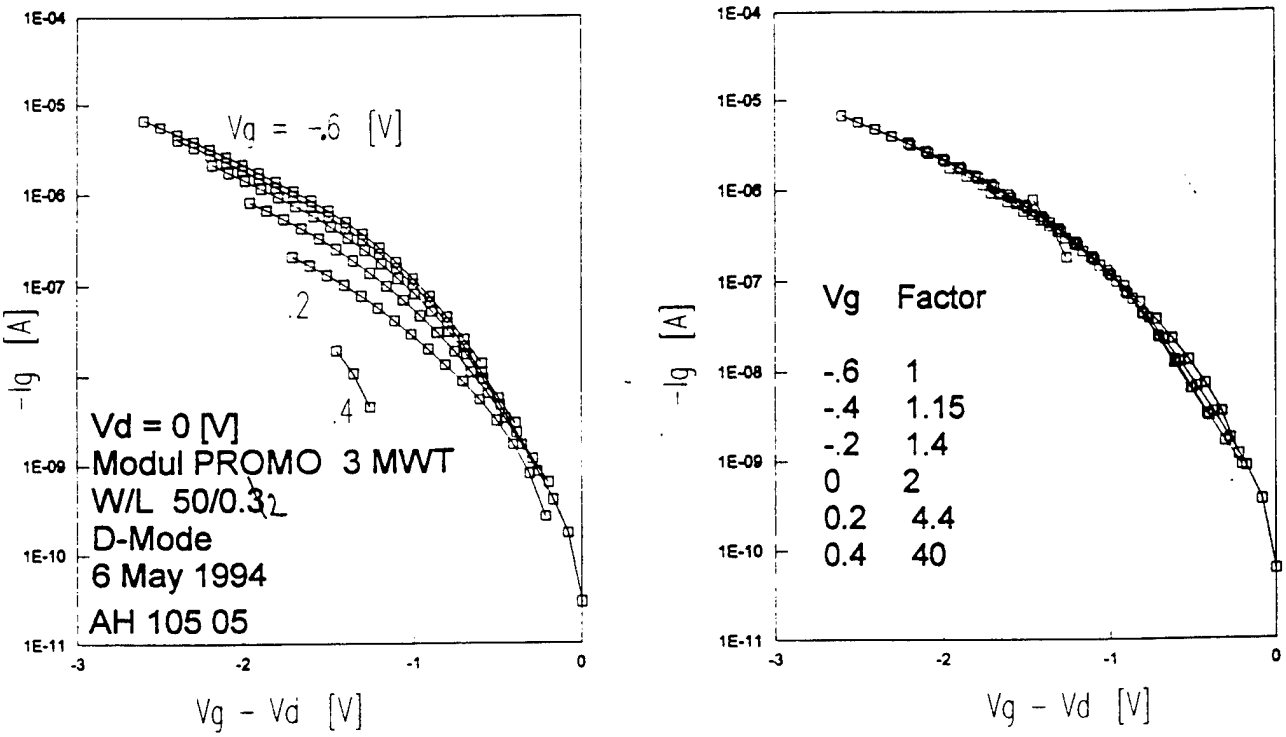

Figure 20 Reverse Gate current Characteristics for a Depletion Mode HFET. The Curves Coincide by Multiplication with the Given Factors

parameter model the gate current is given by

$$i_1 = y_{11}v_1 + y_{12}v_2$$

$$d(i_1)/d(v_2) = y_{12}$$

where i_1 is the gate current, v_2 the drain voltage and y_{12} is the drain transconductance $-G_{gd}$ - jwCgd. Figure 22 presents a typical printout of the equivalent circuit parameters. The specific example measured at a drain voltage of 0.25 V and Vgs of 0.9 V indicate that the Ggd values remain constant over the entire frequency range. These values were measured

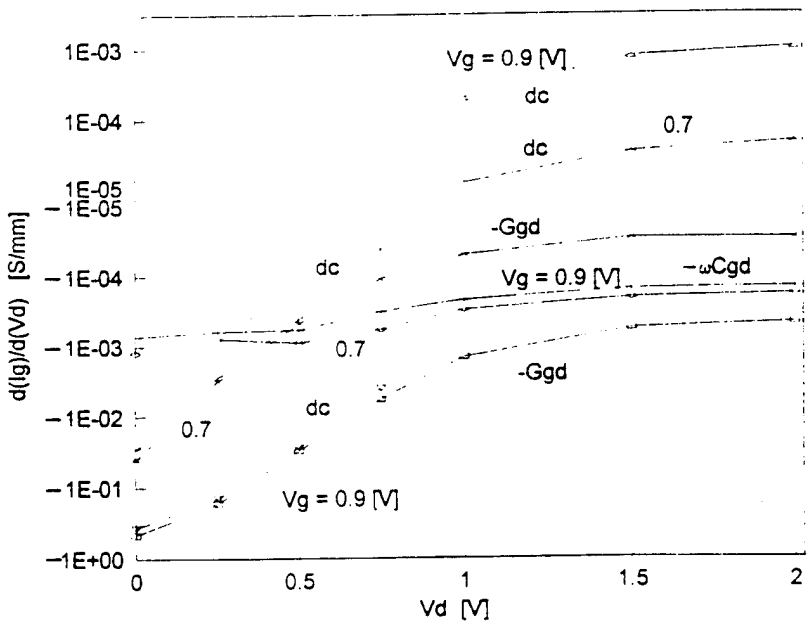

Figure 21 Drain to Gate Transconductance, Measured at dc and rf (100 MHZ).

over a frequency range of approximately 100 kHz to 500 MHZ. The data plotted in Figure 21 were measured t at 100 MHZ. The figure shows an excellent fit between the dc data and the rf data at low drain bias. In this region the absolute values of Ggd are much larger than ωCgd and consequently the latter term can be ignored. At larger drain voltages this condition does not exist and is the reason for the divergence between dc and rf data. Since the dc data can be de-embedded to show the carrier heating effects and since the derivatives of the gate currents with drain voltage coincide at the voltage levels where the carrier heating effects are strong one has to conclude that these carrier heating effects fully follow the input signal up to the measurement frequency of 500 MHZ. The increase in gate current with drain voltage therefore is not due to slow surface leakage effects but the carrier heating effect is probably the correct explanation for the observed effect.

H940221 WAFER 105 VDS=0.25V VGS=0.90V ID=213mA/mm
Width= .05mm No strip
TIMESTAMP: 21 Jul 1994, 11:45:02. WIDTH=.05

Freq GHz	gm mS/mm	Ggs mS/mm	Cgs pF/mm	Cgd pF/mm	Ggd mS/mm	Gds mS/mm	Cds pF/mm	Tau pS	Ft GHz	Fmax GHz	Fgds GHz	Gm/Gds
0.00	20.9	204.5	-2416	1260	162.9	867.5	-9768	---	-0.0	-1.0	.2	.02
.01	26.2	199.0	-21.7	3.165	164.4	869.3	-33.9	-1347	-.2	-1.0	87.4	.03
.02	26.9	198.6	-5.46	.759	164.4	870.2	-23.2	-506	-.9	-1.0	364.8	.03
.03	27.2	198.2	-2.57	1.126	164.7	870.9	-11.2	-333	-3.0	-1.0	246.1	.03
.04	27.3	197.9	-2.56	3.286	165.0	870.9	-6.75	-243	5.9	.2	84.3	.03
.05	27.6	198.0	.07	.755	164.7	871.6	-3.85	-181	5.3	.2	367.7	.03
.06	27.7	197.7	-.74	2.211	165.1	871.7	-2.24	-152	3.0	.1	125.5	.03
.07	27.8	198.2	.80	.486	164.3	870.3	-1.54	-125	3.4	.1	569.7	.03
.08	27.8	197.9	.04	1.560	164.7	870.4	1.62	-111	2.8	.1	177.6	.03
.09	27.9	197.9	.08	1.633	164.7	870.0	.77	-98.0	2.6	.1	169.6	.03
.10	28.0	198.0	.51	1.242	164.7	869.4	-.31	-83.2	2.5	.1	222.8	.03
.11	28.0	198.1	.40	1.255	164.6	868.8	-1.03	-83.2	2.7	.1	220.3	.03
.12	28.1	198.1	.88	.874	164.5	868.1	-3.09	-70.6	2.6	.1	316.3	.03
.13	28.2	198.1	1.05	.627	164.6	868.0	-4.06	-63.3	2.7	.1	440.6	.03
.14	28.2	198.2	1.30	.425	164.5	868.3	-5.49	-57.2	2.6	.1	650.9	.03
.15	28.3	198.1	1.55	.208	164.8	869.3	-6.35	-50.8	2.6	.1	1328	.03
.16	28.4	197.8	1.59	.249	165.0	870.7	-6.08	-50.2	2.5	.1	1112	.03
.17	28.5	197.9	1.53	.384	165.1	871.6	-5.76	-45.9	2.4	.1	721.8	.03
.18	28.6	197.6	1.65	.275	165.3	872.6	-5.63	-43.7	2.4	.1	1011	.03
.19	28.6	197.6	1.57	.440	165.3	873.5	-4.79	-41.9	2.3	.1	632.2	.03
.20	28.6	197.5	1.42	.581	165.3	873.7	-3.24	-35.6	2.3	.1	478.5	.03
.21	28.6	197.6	1.31	.715	165.1	873.4	-2.22	-35.1	2.2	.1	388.8	.03
.22	28.6	197.7	1.32	.707	165.1	872.5	-1.86	-34.8	2.2	.1	392.6	.03
.23	28.7	197.6	1.31	.733	165.1	871.7	-1.29	-32.3	2.2	.1	378.7	.03
.24	28.8	197.9	1.20	.852	164.7	869.8	-1.39	-32.5	2.2	.1	325.1	.03
.25	28.7	198.2	1.20	.771	164.3	868.3	-1.63	-30.8	2.3	.1	358.5	.03
.26	28.8	198.2	1.18	.756	164.4	867.8	-2.01	-30.3	2.4	.1	365.5	.03
.27	28.8	198.3	1.19	.716	164.5	867.3	-2.34	-28.9	2.4	.1	385.7	.03
.28	28.8	198.4	1.31	.586	164.5	867.2	-3.03	-23.4	2.4	.1	471.0	.03
.29	28.7	198.5	1.45	.478	164.3	867.8	-3.77	-22.1	2.4	.1	578.3	.03
.30	28.8	198.4	1.53	.331	164.6	868.6	-4.45	-21.4	2.5	.1	836.3	.03
.31	28.8	198.4	1.58	.344	164.7	869.3	-4.63	-19.3	2.4	.1	805.4	.03
.32	29.0	198.3	1.59	.354	164.9	869.7	-4.49	-20.0	2.4	.1	782.9	.03
.33	29.1	198.4	1.69	.331	164.7	870.1	-4.40	-17.8	2.3	.1	836.6	.03
.34	29.1	198.4	1.66	.397	164.8	870.4	-4.24	-17.8	2.3	.1	698.2	.03
.35	29.3	198.3	1.67	.450	164.7	870.5	-3.84	-19.2	2.2	.1	615.9	.03
.36	29.2	198.2	1.59	.547	164.7	870.5	-3.18	-19.5	2.2	.1	506.4	.03
.37	29.1	198.3	1.46	.680	164.6	870.0	-2.42	-19.1	2.2	.1	407.0	.03
.38	29.0	198.4	1.34	.790	164.3	869.2	-1.98	-20.2	2.2	.1	350.3	.03
.39	29.1	198.4	1.24	.869	164.4	868.3	-1.70	-20.0	2.2	.1	318.0	.03
.40	28.9	198.5	1.14	.900	164.2	867.6	-1.33	-18.9	2.3	.1	306.8	.03
.41	29.1	198.6	1.09	.898	164.2	866.9	-1.42	-18.9	2.3	.1	307.5	.03
.42	29.1	198.6	1.11	.872	164.0	866.3	-1.59	-16.4	2.3	.1	316.2	.03
.43	29.0	198.6	1.16	.750	164.1	866.3	-1.74	-14.9	2.4	.1	367.5	.03
.44	29.0	198.8	1.16	.779	163.8	866.4	-1.79	-13.3	2.4	.1	353.8	.03
.45	29.1	198.9	1.19	.687	164.1	866.7	-1.80	-10.6	2.5	.1	401.7	.03
.46	29.0	198.9	1.19	.708	164.1	867.8	-1.89	-11.8	2.4	.1	390.1	.03
.47	29.0	198.9	1.16	.757	164.3	867.8	-2.00	-12.7	2.4	.1	365.0	.03
.48	29.1	198.9	1.17	.805	164.1	868.5	-1.81	-10.7	2.3	.1	343.6	.03
.49	29.2	199.0	1.11	.861	164.2	868.6	-1.62	-13.8	2.4	.1	321.2	.03

Figure 22 Equivalent Circuit Parameters Obtained from S Parameter Measurements

1.6 Comments and Conclusions

This study revealed many very important results regarding the gate current and the carrier heating effects in HFETs:

1.61 In the IAF HFETs, the carrier heating effect as evidenced by an increase in gate current with drain voltage was masked by the source resistance. De-embedding revealed the carrier heating effects in depletion mode HFETs. Gate currents and carrier heating effects limit the operation of these devices in circuits and must be understood and minimized for improved circuit performance.

1.62 Devices were measured over a wide range of gate lengths and it was observed that at zero drain voltage the gate current scaled with gate length. With drain voltage, the carrier heating effect increased with decreasing gate length. This is an important finding since two opposing effects control the hot carrier current. With decreasing gate length the electric fields in the transistors increase leading to an increased electron temperature and larger emission. Since scattering events are required for the emission of the heated electrons and the scattering length may become comparable to the gate length a decrease in carrier heating effect with decreasing gate length can be predicted. The observed increase of this effect with decreasing gate length clearly requires additional work to minimize gate currents and hot carrier effects.

1.63 The observed result that gate currents do not depend on frequency, measured from dc up to

500 MHZ strongly supports the carrier heating theory. Due to the small thermal mass of the electrons they heat up very fast with delays in the picosecond regime.

1.64 The transition from Schottky barrier to heterobarrier control of the gate current was not observed in any of the IAF HFETs. Not even the InGaAs channel HFETs showed this transition even though the heterobarrier is expected to be more than 200 meV larger than in GaAs channel HFETs. The absents of this transition is probably due to the supply layer charge in the barrier between channel and gate. The expected shift of the threshold voltage due to the InAs content in the channel was observed. For proper operation of these devices in circuits the threshold voltage must be shifted towards more positive values which is achieved by reducing the charge in the supply layers. This offers the opportunity to reduce or eliminate the supply layer in the barrier without the need to increase the supply layer charge beneath the channel. In this case the 1.7 nm n-doped GaAs supply layer can be replaced with an undoped AlGaAs layer with identical thickness. This change may improve the barrier such that heterobarrier control of the gate current is observed.

2. Gate Currents in Heterostructure Field Effect Transistors: Contribution by "Warm" Electrons

2.1 Introduction

Heterostructure field effect transistors (HFETs) find application in digital microelectronic circuits. The enhancement mode HFETs are operated under positive, i.e. forward gate bias and the electrons are confined to the channel by the heterobarrier. In typical HFETs such as InGaAs/AlGaAs/GaAs and InGaAs/InAlAs/InP transistors the height of this heterobarrier is in the range of 300 to 500 meV. The ensuing gate current can be analytically described by tunneling, thermionic emission, or thermionic field emission,[1,2,3,4] depending on temperature and applied gate bias voltage. Experimental observations on GaAs based devices show that the gate current in the subthreshold region is described by the diode equation with an ideality factor close to one and the deduced activation energy represents the barrier height, referenced to the Fermi energy of the source and drain ohmic contacts. Above threshold voltage, the gate current increases with gate voltage due to the increase in Fermi energy within the quantum well, resulting in a reduced effective barrier and a large ideality factor.

Application of a potential to the drain of the HFET has a pronounced effect on the gate current. At small drain voltages the gate current decreases with drain voltage, reaching a minimum at approximately 0.6 V for the GaAs based devices and 0.3 V for the InP HFETs. When the drain voltage is further enlarged, the gate current increases. There

exist several mechanism which may explain the observed characteristics, namely a change in the barrier profile, heating of the electrons by the applied electric field, and band to band transitions. The initial reduction in gate current with drain voltage is attributed to the increase in barrier potential with drain voltage. The increase in gate current at larger drain voltage is due to carrier heating. The aim of this paper is to analyze the carrier heating regime and to determine the degree of heating of the electrons emitted over the barrier in the channel region where the electron emission probability is the highest.

2.2 Theoretical Considerations

It is well known that electrons can be accelerated by an electric field within a semiconductor and become heated or hot. Heiblum[5,6] demonstrated that electrons can traverse the base of an HBT without scattering and arrive as hot electrons at the collector. In HFETs, discussed in this paper, the gate length (typically 1,000 nm) is much larger than the scattering length (several tens of nanometers) and the probability for electrons to scatter as they travel from source to drain is close to one. Nevertheless the channel electrons gain some energy and the two-dimensional electron gas becomes heated due the electric field generated by the drain to source potential. Since the electric field component parallel to the source to drain direction rises with distance from the source, the electron temperature also increases along the channel (Fig. 23, sketch a).

Not only does the electron temperature change along the channel but also the

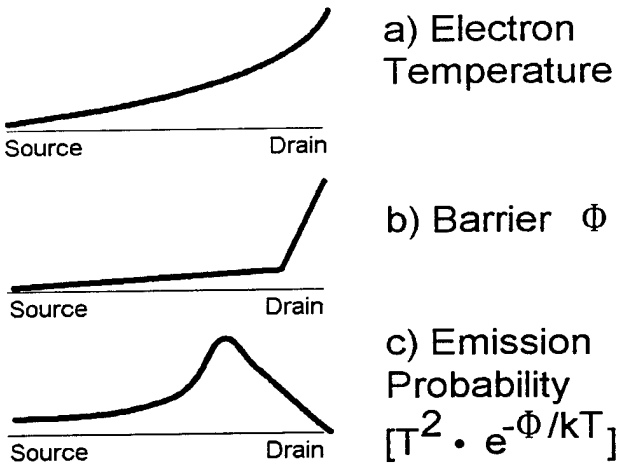

Figure 23 Electron Temperature, Barrier, and Emission Probability

barrier increases from source to drain (Fig. 23, sketch b). At the source side of the channel, the barrier increases slowly towards the drain. At the drain side, in the saturation regime, the increase becomes very steep. The reason for the increase in barrier height is the rise in channel potential, resulting in a decrease in electric field from gate to channel area, which in turn lowers the energy of the eigenstates and reduces the fermi-energy (Fig. 24). At the drain side and at drain voltages larger than the gate voltage, the Schottky barrier rather than the heterobarrier limits the gate current and a more rapid change in barrier height with location is expected. Figure 24c is a three dimensional sketch of the energy configuration from source to drain.

The gate current density along the channel is proportional to $T^2 \bullet e^{\Phi/kT}$ and thisfunction is sketched in Fig. 23c. Neither the electron temperature nor the barrier height are constant along the channel and the gate current density is expected to vary. We assume that the source and drain areas contribute little to the enhanced gate current since near the

source the electron temperature is low and near the drain the barrier height is large.

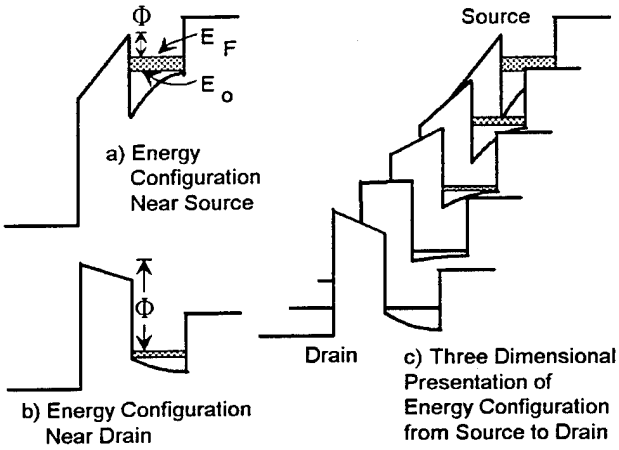

Figure 24 Barrier Configuration

We will restrict the discussions in this paper to the heating of the two-dimensional electron gas by the drain potential. Interband and intraband transitions and their effects on the gate current will not be considered.

2.3 Experiment

In this study both GaAs and InP based enhancement mode HFETs were investigated. The material was grown by MBE on semi-insulating GaAs or InP substrates. The GaAs based structures consist of a 15 nm InGaAs channel layer with 18% InAs content and a 25 nm AlGaAs barrier layer with 75% AlAs content. The high AlAs mole fraction was chosen to optimize the p-HFET devices, used in the complementary HFET process. Figure 25 is a schematic of the InGaAs/AlGaAs/GaAs HFET. A WSi refractory gate was used to allow self-alignment of source and drain by ion implantation. A sidewall spacer

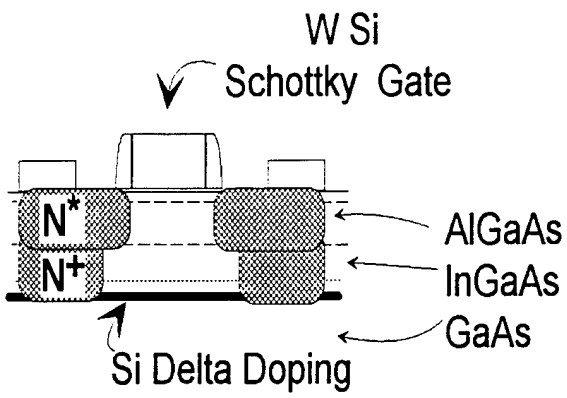

Figure 25 Device Structure

to the gate minimized the overlap of the gate and the implanted areas. The InP based HFETs had a similar structure with a 3 nm $Al_{0.5}Ga_{0.5}As$ cap layer followed by a 30 nm $In_{0.52}Al_{0.48}As$ barrier layer and a 25 nm $In_{0.53}Ga_{0.47}As$ channel.

The devices were packaged and were tested in a temperature controlledchamber. The current and voltage measurements were collected with an HP 4145B Parameter Analyzer. Figure 26 presents a typical gate current vs. gate voltage characteristics with both source and drain grounded. At low gate voltages the current is described by the

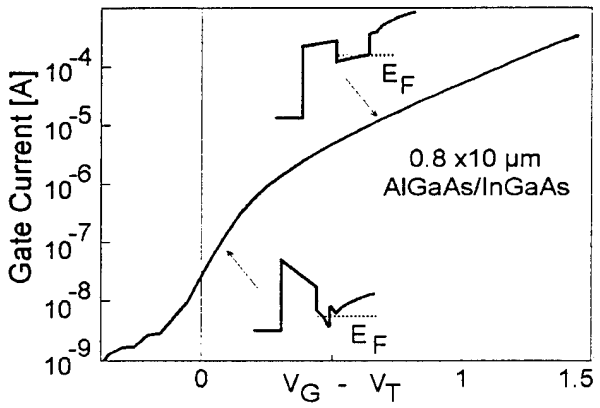

Figure 26 Gate Current vs. Gate Voltage

thermionic emission equation with an n- value of approximately one since the Schottky barrier controls and limits the gate current in this regime. At higher gate bias voltages the slope of the curve becomes smaller resulting in an n- value of close to ten. The reason for the increased n- value is that in this regime the gate current is limited by the heterobarrier and the effective barrier height changes slowly with gate voltage.

The gate current not only depends on the gate but also on the drain bias voltages. Figure 27 presents gate current of an InP based HFET vs. drain voltage for various

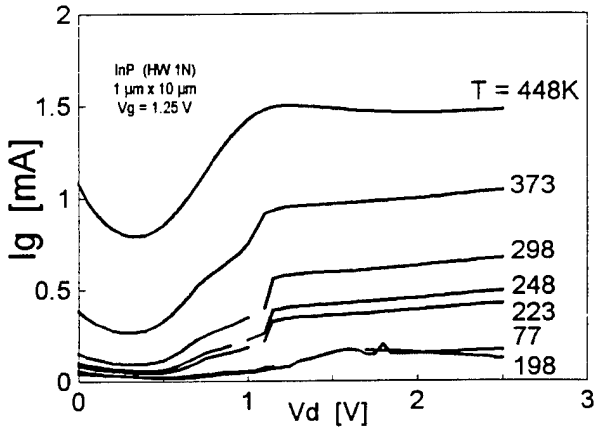

Figure 27 Gate Current vs. Drain Voltage

temperatures. Similar results are obtained on GaAs based HFETs. The data show an initial decrease in gate current with drain voltage. Above a drain voltage of approximately 0.3 V one observes an increase in gate current and the curves typically show a step like increase. Figure 28 presents the normalized gate current for a 0.8 µm gate length device for different temperatures. The graph indicates that the gate currentdependence on drain voltage is minimal at low temperatures. Figure 29 is a graph of gate current vs.

temperature for two gate voltages and three drain potentials. One observes that a drain potential of 1 V shifts the gate current characteristics to lower temperatures by approximately 50 to 70 °C.

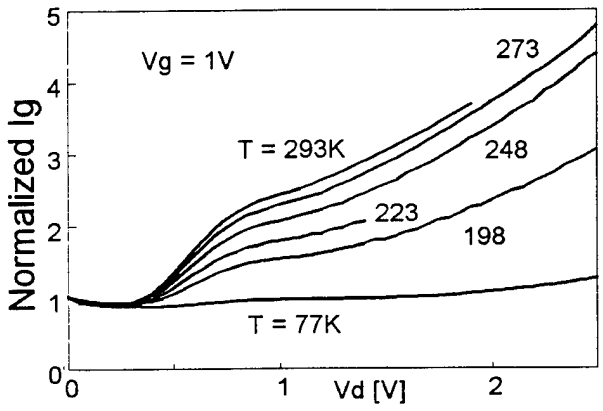

Figure 28 Normalized Gate Current

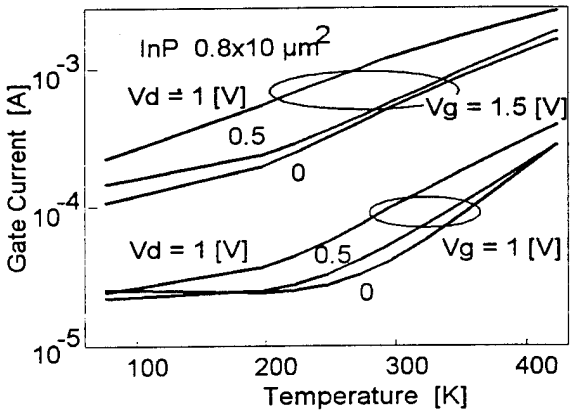

Figure 29 Gate Current vs Temperature

2.4 Discussions

In this section, emphasis is placed on the effect of drain voltage on gate current. Figure 27 shows the previously reported initial decrease in gate current with drain voltage, reaching a minimum at approximately 0.3 V for InP based devices. The drain voltage at the minimum for the GaAs based devices is 100 percent larger than that observed in InP based devices. The decrease in gate current is caused by the increase in barrier height with drain voltage. When the gate voltage is further increased one observes a steep rise in gate current due to heating of the two dimensional electron gas by the drain potential. It is interesting to explore the approximate temperature of the electron gas. Figure 28 clearly shows that the emission of heated electron is temperature dependent. The electron heating effect at 77 K at 1 V gate bias is not strong enough to overcome the increase in the barrier height with drain bias and contributes little to the gate current. Nevertheless even at 77 K the gate current does not decrease with the drain bias as it should have if the electrons contributing to the gate current remain cold. At 77 K it is difficult to estimate the electron temperature increase for the electrons contributing to the gate current since tunneling plays an important, if not dominant role. However at higher temperatures, the average increase in temperature of the emitted electrons can be estimated from Fig. 29. One observes that a drain voltage of 1 V shifts the gate current characteristics to lower temperatures by 50 to 70 °C. As discussed above, a drain potential increases the electron temperature and also elevates the barrier for the two-dimensional electron gas along the channel. The increase

in electron temperature raises the gate current and shifts the gate current characteristics towards lower temperatures. The enlargement of the barrier lowers the gate current and shifts the characteristics towards higher temperatures. Hence the increase in electron temperature is larger than the 50 to 70 °C shift in gate current characteristics. The following is an estimate of the contributions of these two mechanism. The increase in channel potential with drain voltage is limited to 300 mV due to the saturation velocity in GaAs and InGaAs. The increase in barrier height Φ due to the 300 mV channel potential is estimated to be $\Delta\Phi$ = 50 meV considering the large ideality factor of approximately 10 of the diode characteristics at this gate voltage. Assuming an increase in the barrier height Φ from 300 to 350 meV and increase in electron temperature T by 100 °C from 300 to 400 K due to a 1 V drain potential the thermionic emission equation

$$Ig = A \bullet T^2 \bullet e^{-(\Phi/kT)}$$

where A is a constant, results in

$$\frac{Ig(Vd=1)}{Ig(Vd=0)} = 8.$$

This increase in gate current is consistent with the experimental results and indicates a rise in electron temperature of approximately 70 to 100 °C. As indicated in Fig. 23, the temperature of the two-dimensional electron gas increases towards the drain and

temperatures much above the observed values are expected at the drain side of the channel. However these hot electrons contribute to the gate current marginally because the barrier increases rapidly towards the drain, offsetting the increased electron temperature. The experimental data suggest that neither source nor drain areas contribute significantly to the gate currents under drain bias but that "warm" electrons from an area away from source and drain are the cause for the observed currents.

3 Photoelectric measurements of interband transitions in fully fabricated pseudomorphic high electron mobility transistors

3.1 Introduction

Optical techniques such as photoluminescence and photoreflectancehave been commonly used to measure the energy band profile of modulation-doped quantum well structures and pseudomorphic high electron mobility transistors (PHEMTs).[7,8,9,10,11,12] These techniques provide information on the epitaxial layers *before* device processing and sample over areas that are typically much larger than the final device dimensions. Unfortunately, because of processing effects and applied voltages, the band profile of the final *fabricated* device can be dramatically different from that of the virgin epitaxial layer structure. For example, the Schottky gate metal pins the Fermi level at the surface, altering the internal field distribution in the structure. Knowledge of the band profile in fabricated transistors is critical for investigating the effects of the epitaxial layer structure on device performance. Photoelectric techniques such as photoemission and conduction (PEC) sense electrical currents within a device resulting from optical excitation. Because of the localization of the currents and the precision with which they can be measured, these techniques are well-suited to obtain barrier heights and bandgap information on small devices. Previous photoelectric device studies used front side illumination and required thinned metal gates,[13,14,15,16,17] entailing extra processing and making the characterization technique destructive. Attempts to use backside illumination were limited by above-bandgap

absorption in the substrate. Fortunately, the interband energies in the PHEMT channel are significantly smaller than the substrate bandgap. Consequently, light incident on the backside can reach the channel, permitting photoelectric studies on fully fabricated devices.[18] The ability to measure both optical properties and microwave performance on the same device provides a unique opportunity to connect variations in transistor behavior to changes in material structure and quality.

In this paper we describe the PEC measurement technique and report photoconduction (PC) measurements on fully fabricated PHEMTs with 1 μm gates grown on GaAs substrates. The qualitative shape and bias dependence of the observed PC spectra can be reproduced by a simple model. For samples where all dopants lie between the gate and the well, the experiments and calculations suggest that the $\Delta n=0$ selection rules for square-well interband transitions are strong for gate biases near pinch-off. Therefore, by comparison with a model the interband transition energies can be identified. At lower biases, where there is significant charge in the well, the selection rules are weak. For samples with dopants both above and beneath the well, however, the selection rules are not strong at any bias.

3.2 HEMT fabrication

The heterostructure material was grown by MBE. The devices were fabricated on two wafers with distinct layer structures. Wafer 1 nominally consists of the following layers:

35 nm GaAs with $5x10^{18}$ cm^{-3} Si doping, 3 nm AlAs etch stop, 20 nm $Al_{0.24}Ga_{0.76}As$ barrier with $5x10^{17}$ cm^{-3} Si doping, $4x10^{12}$ cm^{-2} delta doping, 4 nm $Al_{0.24}Ga_{0.76}As$ spacer, 12.5 nm $In_{0.22}Ga_{0.78}As$ channel, 489 nm GaAs buffer, and an 11 period superlattice. We refer to Wafer 2 as an underdoped structure since it is nominally identical to Wafer 1 except for an additional 10 nm $1x10^{18}$ cm^{-3} Si-doped GaAs layer located 3 nm below the well.

The PHEMTs were isolated on the wafer by masking the active areas using standard photolithographic techniques and by forming mesas via wet etching 170 nm down to the undoped GaAs buffer region using $HF:H_2O_2:H_2O$ at (1:1:8). Drain and source ohmic contacts were formed using the metal lift-off technique with standard AuGe/Ni metal evaporation, and were alloyed at 450 °C for 30 seconds using rapid thermal annealing. The ohmic contacts were electrically tested, yielding a contact resistance of 0.060 Ω-mm, a specific contact resistance of $1.73x10^{-7}$ Ω/cm^2, and a sheet resistance of 191 Ω/square. Next, the gate contact was formed using optical lithography to define the gate region, and the top GaAs ohmic contact layer was removed before gate metallization using a citric acid:H_2O_2 selective etch which stops at the AlAs etch stop layer[19] Then the AlAs etch stop layer was removed prior to metallization using $HCl:H_2O$ (1:10). The gate contact was formed by metal lift-off of evaporated 20 nm Ti/580 nm Au metal, giving 1 μm gate length PHEMT devices with 5 μm source/drain spacing. A final metallization of 20 nm Ti/980 nm Au was then deposited to connect the source and drain to probe pads. Three device configurations were tested. Devices A and B are 2-finger FETs and device C is a 6-finger FET, all with 100 μm unit gate width. Devices B and C have ohmic metal only on the mesa top with final

metal connecting the ohmic metal to probe pads. Device A has probe pads and interconnecting metal defined in the ohmic layer to allow testing of this device during gate recess and immediately following gate deposition.

3.3. Experimental techniques

Figure 30 presents a sketch of the experimental setup. The PEC measurements are performed on-wafer at room temperature using either Cascade or shielded Pico probes. The wafer chuck contains a hole in its center. A micromanipulator positions one end of an optical fiber directly underneath a device, and the other end of the optical fiber is

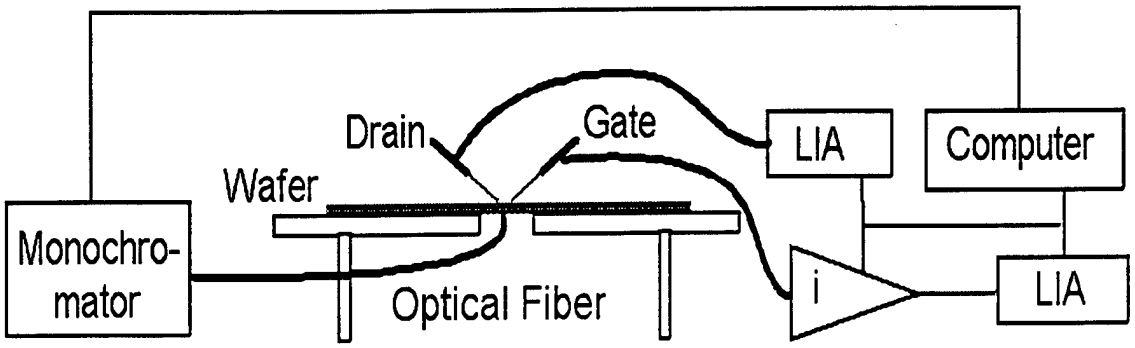

Figure 30 Experimental setup for PEC measurements

connected to the exit slit of a SpectraPro-150 (Acton Research Corporation) monochromator. A 50 W tungsten light source is employed and the light is mechanically chopped. Stanford Research SR530 lockin amplifiers are employed to measure the photocurrents at the drain and gate electrodes. A low noise current preamplifier SR570 is

used to amplify the gate photocurrent and to provide the gate voltage.

3.4 Theory

We have successfully modeled the PC spectra for Wafer 1 by assuming that the photocurrent is proportional to the interband optical absorption coefficient of the channel. The absorption coefficient calculation is performed in three steps: First, the electron charge distribution and band profile are obtained for a given gate bias using a self-consistent Schrödinger-Poisson solution. In the region surrounding the delta-doping and the InGaAs channel, the electron effective mass equation is solved by finite-difference methods and the electron density is obtained from the resulting wave functions; in the remainder of the device the electron density is obtained semi-classically. We calibrate the model for Wafer 1 by adjusting the Schottky barrier on the AlGaAs barrier layer until the calculated pinch-off voltage agrees with experiment. (The underdoping in Wafer 2 created instabilities in the self-consistent Poisson-Schrödinger solution. Since the model would not converge for large voltages it was not possible to model Wafer 2.) Next, using the self-consistent band profile, valence subband energies and wavefunctions are obtained by solution of the 4x4 strain-dependent effective mass equation. Finally, the absorption coefficient for normally incident light is calculated from wave function overlaps with state occupation determined by the self-consistent Fermi level.

In flat (square) quantum wells, the interband absorption coefficient reflects the

canonical $\Delta n=0$ selection rules and sharp steps appear at the corresponding energy separations E1-HH1, E2-HH2, etc. Here En represents the n'th electron subband, and HHm represents the m'th heavy-hole subband. If the band-edge profile of the well is sharply bent or tilted – as when there is significant charge in the well or a large electric field across the well – then the selection "rules" are not as strong, and each hole subband couples strongly to all electron subbands. In this case the absorption curve consists of many small, closely-spaced steps, and the sharp $\Delta n=0$ transitions do not predominate.

In Figure 31 we show the calculated absorption coefficient for the nominal structure of Wafer 1 at room temperature. The solid curve is calculated for the theoretical pinch-off

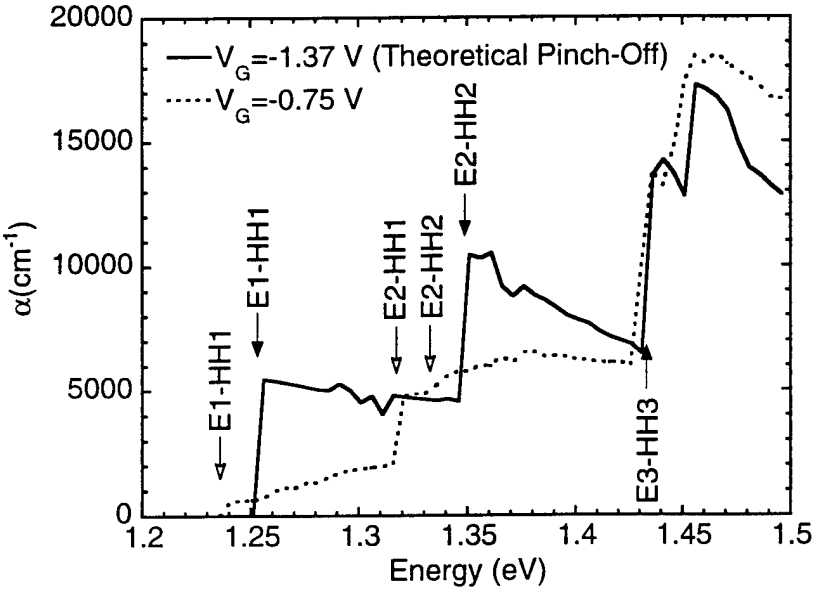

Figure 31 Calculated absorption spectra for interband transitions for pinch-off (solid curve, solid arrows) and "on" (dotted curve, open arrows) conditions

voltage, where the quantum well is essentially devoid of charge. Since Wafer 1 has no

underdoping, there is no ancillary space-charge field across the channel. Therefore, the pinched-off well is essentially flat, the selection rules are strong, and the absorption spectrum exhibits a few large, sharp steps only at the $\Delta n=0$ transition energies. The dotted curve, by contrast, is calculated at 0.62 volts above pinch-off. At this gate voltage there *exists* substantial channel charge and there is substantial band-bending in the well. Hence the selection rules are weak, and smaller, more numerous steps are observed corresponding to interband transitions that do not conserve subband number. In addition, the low energy absorption is substantially reduced because the first electron subband lies below the Fermi level.

3.5 Experimental results

In Figures 32-35 we show several examples of measured photoconduction (PC) spectra for devices A, B and C; we also present differentiated PC spectra to more clearly define the interband transition energies. The photocurrents are all measured with a source-drain voltage of 20 mV and are normalized for constant photon flux. Many devices were tested and the data are reproducible.

In Figure 32, we present PC data for device A fabricated on Wafer 1 at two different gate biases. Figure 32(a) shows data at pinch-off (-1.5 V for this device), and the spectrum shows sharp steps. The corresponding peaks in the differentiated PC spectrum at 1.19 and

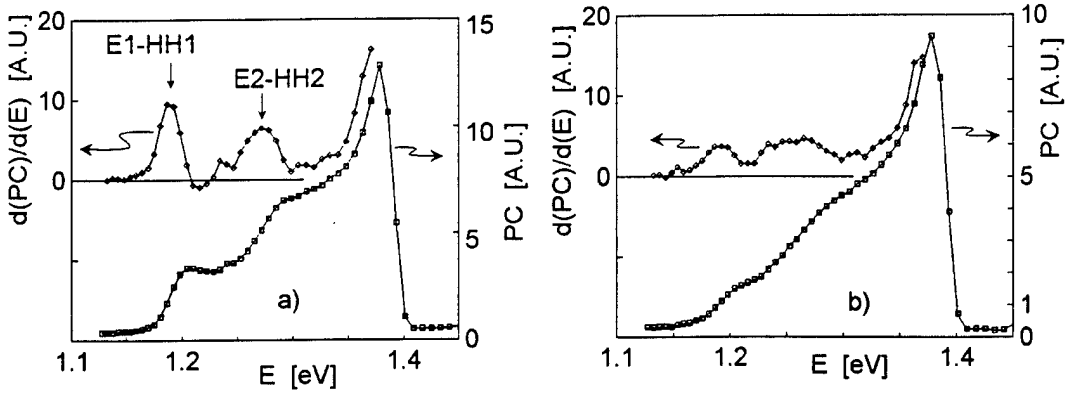

Figure 32 Experimental photoconduction and derivative curves for Wafer 1, Device A, at (a) pinch-off (Vg=-1.5 V) and (b) "on" (Vg=-1 V) conditions

1.28 eV are attributed to the E1-HH1 and E2-HH2 transitions, respectively, since the shape agrees with the model curve in Figure 31. The peak separation also agrees well with the model but the absolute values are lower; this rigid shift may result because the layer thicknesses or compositions differ from the nominal values. The sharp rise in the PC spectrum near 1.35eV may mark the onset of the third step seen in the calculated curve of Figure 31, but a transition energy cannot be clearly estimated because of the nearby GaAs substrate absorption. The Figure 32(b) data were taken at a gate bias of -1 V where the channel contains a significant amount of charge. Here, by contrast, the sharp steps are washed out and the PC spectrum is relatively featureless. This is consistent with the weakening of selection rules discussed in Section 3.4. Figure 33 presents a PC spectrum for device B immediately adjacent to device A. This data, taken at pinch-off, shows two sharp steps similar to the device A spectrum in Figure 32(a). However, the rise in PC at photon energies above 1.35 eV is missing. The reason for this pronounced difference is not known. Recall that devices A and B differ only in the gate electrode layout and

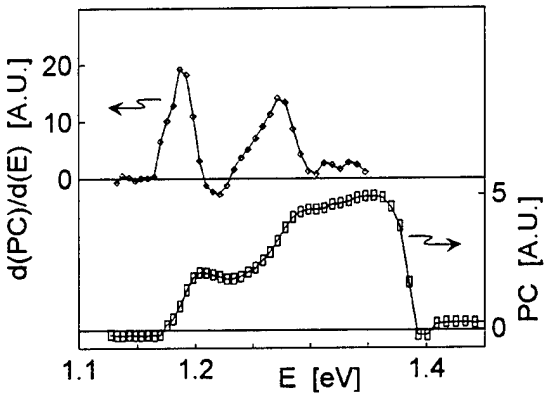

Figure 33 Photoconduction and derivative of Device B on Wafer 1, at Vg=-1.5 V (pinch-off)

metallization; the epitaxial layer structures are identical.

Figure 34 shows a PC spectrum for device C fabricated on Wafer 2 which contains underdoping. The observed PC spectra, even when measured at pinch-off as shown here, lack distinct steps. We attribute this behavior to the underdoping donors. Because of the

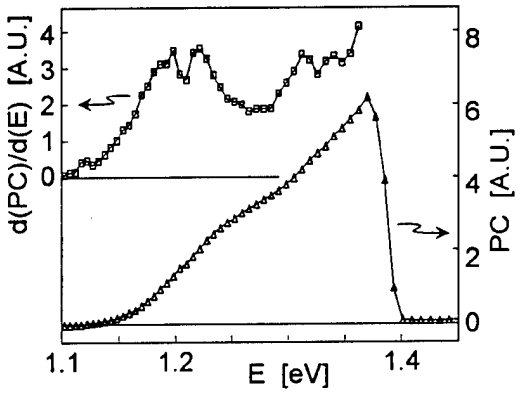

Figure 34 Photoconduction and derivative of Device C on Wafer 2 (underdoping), at Vg=-2.3 V (pinch-off)

extra fixed charge underneath the channel, the well profile exhibits significant band tilting

even when the channel is depleted. Consequently, the interband selection rules are weakened at all biases.

3.6 Conclusions

We present experimental photoconduction results that allow direct observation of channel interband transitions at room temperature on fully fabricated PHEMTs. For devices *without* underdoping, the photoconductivity spectra depend dramatically on gate bias. At pinch-off the spectra show strong, sharp steps, while at more positive biases the sharp structure is washed out. This behavior can be qualitatively reproduced with a simple model that assumes proportionality between the photoconductivity and the interband absorption. The bias dependence predicted by the model results from changes in the strength of the $\Delta n=0$ selection rule. Devices *with* underdoping, however, show broad, relatively featureless PC spectra at all biases because the fixed charge under the well tilts the bandedge profile even at pinch-off.

4 Acknowledgement

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